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Issue 5

Generate complex MIMO signals at up to 6 GHz Page 10

SoC FPGAs COMBINE PERFORMANCE & FLEXIBILITY

Page 16

EDN europe

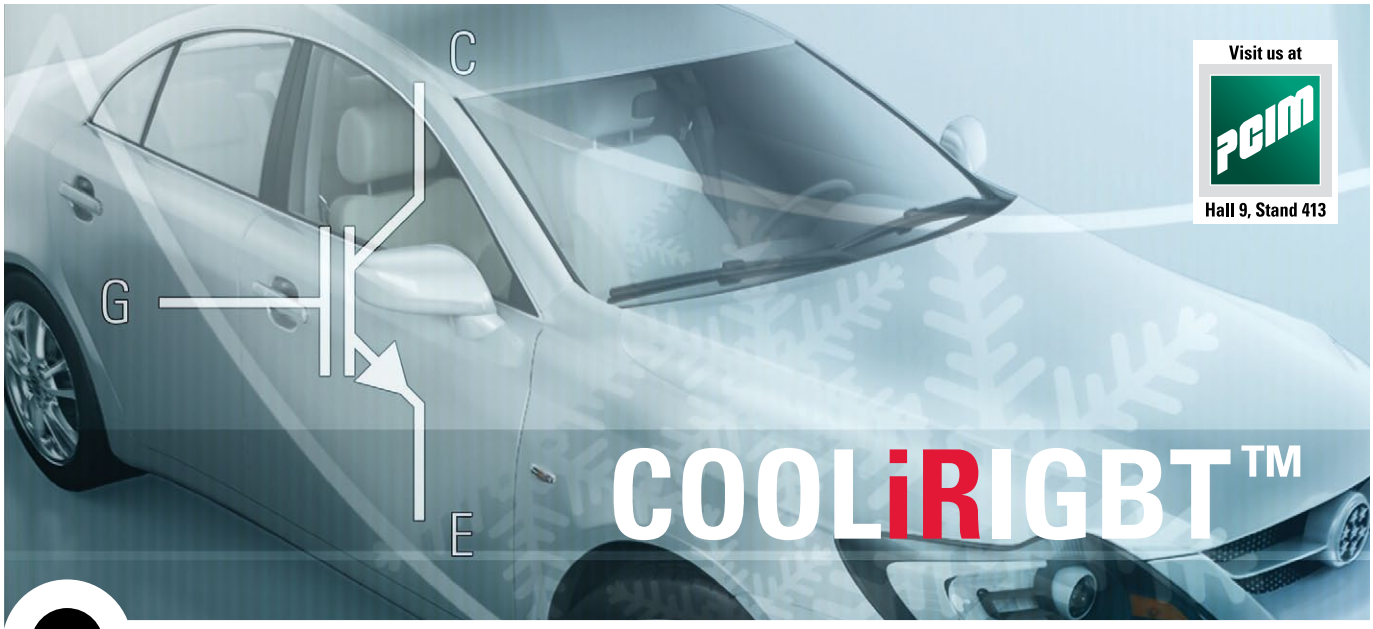
contents

May 2013

DEPARTMENTS & COLUMNS

DESIGNIDEAS

pulse



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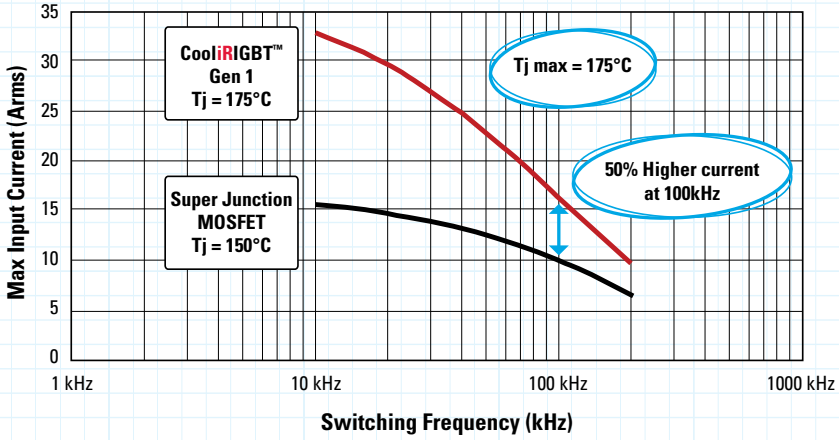

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Hit the switch

There is a newspaper in the UK called the Daily Mail; and its companion title, the Mail on Sunday. Its political stance, I believe it's fair to say, is on the right of centre. Its style inclines to – let's not call it sensationalism – say, rather, to finding something alarming in almost any aspect of the news or, indeed, of modern life. Its readers – who appear to be very happy with the arrangement – are fed a constant diet of topics that they told they ought to be very angry about. Hold that thought, and please don't skip ahead in the text – there is a point to emerge.

We are all familiar with the concept of the smart grid. Many readers of this column will be concerned with developing products that will, in time, bring about the smart grid. The peak-to-average ratio (to borrow a metric from another sphere of technology altogether) of power generation is a serious constraint. The grid can, and does, impose step changes in demand that cannot possibly be met by the response time of (most) generating plant – conventional or thermal alike. Plant must therefore be run with capacity in reserve to meet all likely peaks, which is inefficient and, in an era in which "you can't be too green", less and less acceptable.

Long-established practices such as low-cost night-time tariffs were an attempt to smooth some of the longer-period peaks, but the smart grid will work on a shorter timescale. A proportion of the demand on the power grid feeds intermittent loads that are relatively insensitive to the detail of their duty cycles. Loads such as refrigeration, with long time-constants on the thermal side of the equation, may be indifferent to whether they are on or off for a few minutes in this hour, or in the next hour.

So the technologies with which we are all familiar – Zigbee, EnOcean or some other wireless mesh networking, or power line communications; a few extra lines of code in the appliance's microcontroller; solid-state switching of all loads; data concentrators, servers and some modelling of the network and its responses – all of these, as we know, will enable the grid to trim the peaks from the load, and better match base-load power generation to average demand. The consumer who gives the grid access to their smart appliances should expect to get a more favourable tariff in return. It will, or should, be a classic "win-win".

It takes, therefore, a particularly paranoid mindset, a fundamentalist distrust of all the works of any form of officialdom, to manufacture out of the first moves towards the smart grid, a page-one headline on a Sunday newspaper – and here I must resort to cliché and affirm that I am not making this up – that declares, "Big Brother to switch off your fridge". Or, you might conclude, considerable desperation in the search for a better leading story.

In reality, domestic appliances – even aggregated – probably won't make very much difference, but neither is their network connection inherently sinister. It's easy to mock this sort of thing and, as you can tell, have a good deal of fun in so doing. But it does remind us of the fact that, if those with an engineering mindset and training are not ready to speak up and add informed commentary, then the uninformed will have free rein. This, naturally, works both ways. If we challenge paranoia about power-company-controlled fridges, we should also be ready to point out the dangers inherent in other developments that conceal real but less understood hazards. Have you any candidates to suggest? Do you see any technology developments that the industry is currently working on where the possible hazards might outweigh the potential, or intended, benefits?

pulse

xCORE industrial multicore microcontrollers gain analogue functions

XMOS has added a number of analogue functions to its multicore MCUs; integrated analogue functions will reduce component count, save power, and improve signal integrity, allowing you to combine analogue and digital interfacing, communications and deterministic control in a single device. xCORE-Analog is a range of 6, 8, 10, 12 and 16-core multicore microcontrollers that XMOS configured fordesigners of industrial products.

With an integrated analogue-to-digital converter, power management circuitry and a range of timers, the xCORE-Analog or 'A-Series' devices will be used in a range of industrial applications such as interfaces, high-level sensors and actuators, PLCs, communications devices and motor controllers.

Developers can use a level of multicore computation resource scaled to their exact requirements.

A-Series chips include up to eight channels of 12-bit, 1 Msample/sec A/D conversion; power-on reset, brown-out protection and watchdog facilities; integrated oscillator; deep-sleep memory; and integrated DC/DC converter. You can reduce external component-counts and implement designs using simple two-layer printed circuit boards. The devices' power management features enable low sleep-mode power consumption of 100 µA.

The introduction of the A-Series follows several recent announcements from XMOS in the industrial arena, including the addition of industrial Fieldbus capabilities; the launch of an industrial serial bus (IS-BUS) I/O card for the modular sliceKIT development system; and the announcement of a collaboration with Synapticon enabling smart motor control and service robotics applications. The A-Series is supplemented by the xSOFTip range of soft peripherals, which includes real-time Ethernet, USB and human-machine interface (HMI) functions.

As with the pure-logic XMOS products, a major claim for the A-Series is timing predictability; it also brings the extremely low latency and hardware-level responsiveness of xCORE multicore microcontrollers to developers working on any type of system that needs to interface with analogue signals. Like the existing xCORE-General Purpose (L-Series) and xCORE-USB (U-Series) product ranges, the A-Series is configured and programmed via the xTIMEcomposer Studio development toolset, a C-based design environment that is timing-aware, allowing you to interface with hundreds of different types of sensors at the front end. xCORE A-Series devices will be sampling in Q2 2013, with volume production expected in Q4. Pricing is from $4.60 (25k+).

XMOS; www.xmos.com or for distribution sources, www.xmos.com/contact/distributors

XMOS' multicore, deterministic MCUs now have analogue functions on-chip

Single-chip touch control for Windows 8 tablets

Atmel has extended its maxTouch range of touch controller ICs with the T-series. With high volumes of touch products being marketed in smartphone/handset and tablet formats, Atmel has optimised this product for that sector. The mXT2952T is, according to Rob Frizzell, Director Touch Product Marketing in Atmel, mXT2952T: the first ultra low-power, single chip, capacitive touch solution for Windows 8 certified 15.6-in. displays. This conforms to the Windows 8 specification of up to 15.6 inch – but you can control an larger touch screen under Linux or Android, Frizzell says. The series offers solutions for screens of 3 to 23 inches. The company has incorporated several of the features it has developed for existing Atmel touch products. You can use the maxStylus (on screens of up to 13.3 in.), an active stylus that interacts with the touch sensing matrix without the need for an extra sensor layer; the maxFusion SensorHub integrates motion and sensory controls; and the Xsense technology supports the use of flexible and "edgeless" - or frameless – displays.

The maxTouch T uses dual mutual- and self-capacitance sensing, claimed to give the best performance in terms of power, noise immunity, glove-touch sensitivity, moisture-insensitivity and latency. It handles 2952 nodes, has a refresh rate of over 150 Hz, can track at over 60 inches per second, and track 10 touches at over 100 Hz with full noise avoidance. Latency is under 10 msec.

You can use fine-line-metal (FLM) screen technology as well as ITO overlays, and a 32-bit AVR-derived microcontroller filters noise, computes multi-touch points, and eliminates false responses.

The mXT2952T replaces a 3-chip set to achieve similar results, occupies a 5 x 10 mm package and could yield a functional outline of 6 mm wide by 80 mm long to fit within a typical portable product build. Frizzell estimates a cost reduction over the 3-chip solution of around 2x.

Atmel, www.atmel.com

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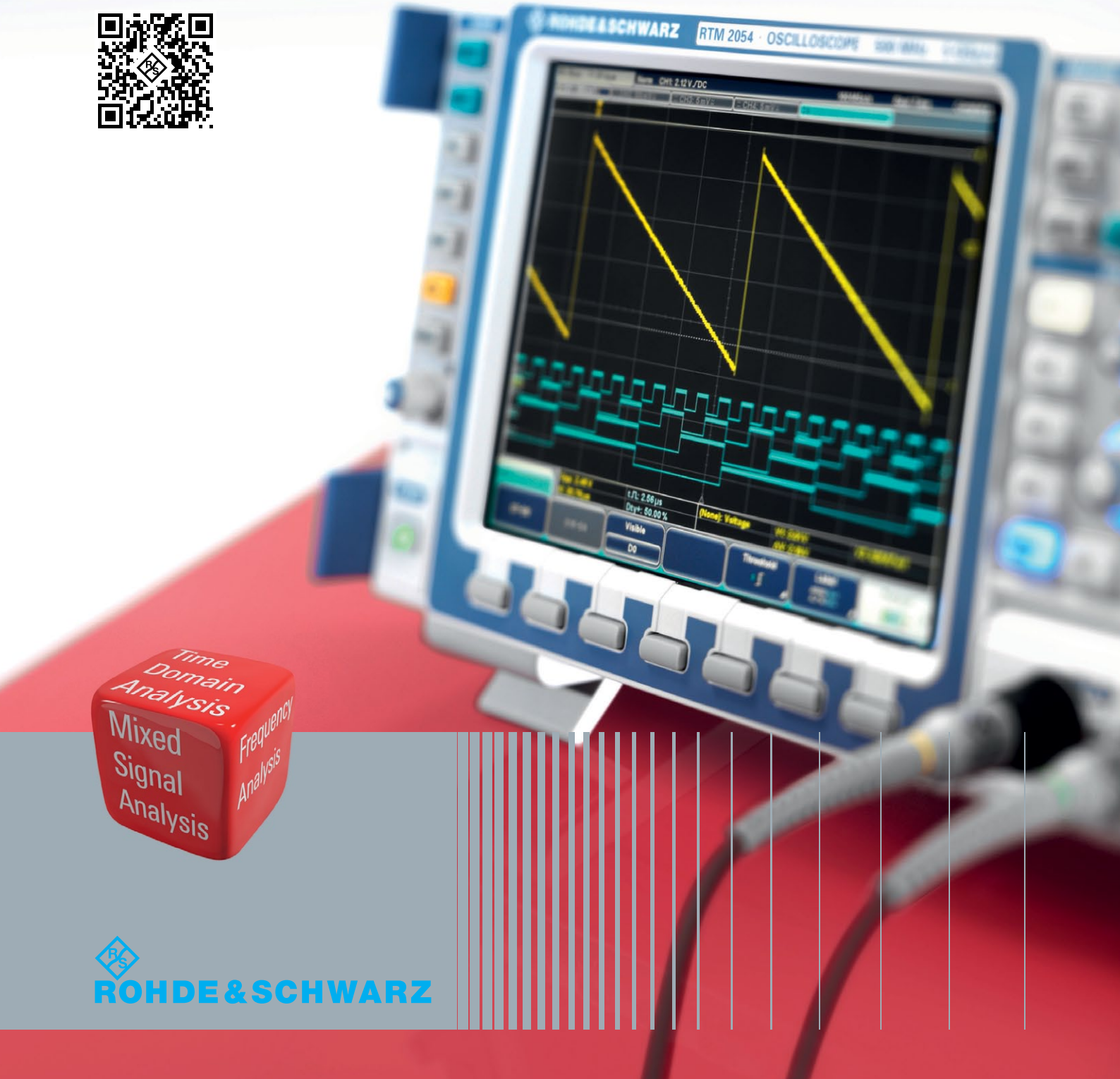
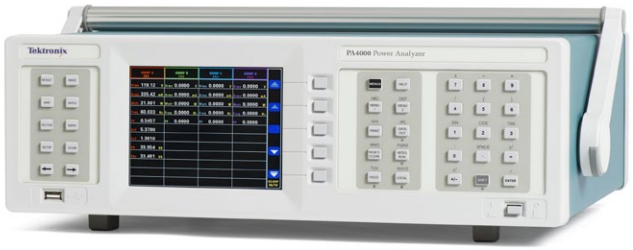


ROHDE&SCHWARZ

Tek builds on Voltech acquisition with power analyser launch



The PA4000 handles up to 30A and identifies harmonic components up to the 100th harmonic.

Earlier this year Tektronix acquired the power-analyser product line and intellectual property, in that speciality, of Voltech. Now, bringing to market a project that was under way at Voltech, Tek has introduced the PA4000 Precision Multi-Phase Power Analyser, offering power electronics engineers high levels of measurement accuracy on real-world signals. A key piece of technology is the current shunt employed in the analyser, which is termed the Spiral Shunt: this design confers stability in measurements as it remains constant over load and temperature, including self-heating effects, in terms of the resistance it presents. This, Tek says, gives power electronics engineers stable, precise current measurements even on highly distorted power waveforms common in many applications.
Tek presents the PA4000 as being complementary, in making power measurements, to its existing oscilloscope and probe range. A high proportion of scope users are also power analyser users, the company found, prompting its move to add the product line. Scopes will look at individual functions within a power system; the analyser will monitor end-to-end. You can use the unit to measure for conformance to regulatory standards today and in the future; it has application-specific test modes and a full set of standard features including communication interfaces and PC-based software. Key industries include motor drives, electric propulsion, backup power, alternative energy, and high-efficiency lighting. Many of these engineers work on designs that are subject to government regulations and customer requirements that dictate efficiency and the amount of harmonic distortion or other "line pollution" that may be imposed on the power grid. The PA4000 features precisely-matched inputs, wide input ranges and advanced signal processing to deliver consistently high measurement accuracy in all types of measurement environments.
A particularly difficult challenge due to the rise of new higher-performance technologies is obtaining consistently high measurement accuracy. The PA4000 uses two Spiral Shunts on each channel – one for current measurements up to 1A, for precise low-current measurements, and one for current measurements up to 30A, for higher-current measurements. This shunt design is then combined with high-speed digital signal processing algorithms, allowing the PA4000 to track power cycles accurately, in the presence of transients and noise.
To save engineers setup time and reduce errors, the PA4000 offers a set of application-specific measurement modes such as standby current, motor drive and ballast. The analysers provide LAN, USB, and RS-232 interfaces as well as harmonics measurement capability up to the 100th harmonic. In addition, software for controlling the analyser, downloading measurements, and logging on a PC is also included in the package. The PA4000 Power Analyser has a starting price €8,350.
Tektronix, www.tektronix.com

USB 2.0 interface, coax physical layer on MOST150 network chip

Microchip has announced a MOST150 Intelligent Network Interface Controller (INIC) with a USB 2.0 high-speed device port and an integrated coax transceiver. According to Rainer Klos, Vice President Systems and Solutions at Micochip AIS, the move brings the multipurpose interface functionality of the USB into the MOST environment, and provides the co-axial cable interface that many car makers are developing for high data-rate traffic. The OS81118 allows you, for example, to create in-car mobile and Wi-Fi connectivity applications on the MOST150 network by connecting a standard Wi-Fi/3G/LTE module via USB. This solution reflects today's market demands for consumer applications within the automotive environment, such as Internet access, e-mail, social networking and local services. It reflects, Klos says, the prevalence of the USB interface on system-on-chip ICs (SoCs) and ASSPs and supports the trend in the infotainment market to use high-end SoCs, developed for consumer and mobile devices, within automotive applications. However, those SoCs have no automotive-specific interfaces, such as CAN, LIN, MediaLB or MOST; the OS81118 enables automotive engineers to connect up-to-date multi-core consumer SoCs to in-vehicle MOST networks. Besides the optical physical layer (oPHY) interface, the OS81118's coax transceiver opens a cost-reduction path on the MOST physical layer. Additionally, this coaxial physical layer (cPHY) could be used for Advanced Driver Assistance Systems (ADAS). For the developer, the device is a MOST controller that – from the point of view of the traffic and data content – looks like a USB device (both for audio and packet-data traffic): the developer does not need an in-depth knowledge of MOST to use it. Similarly, Klos points out, the operating systems also does not need to know about MOST. You can create a bridge from deeply-embedded functions to a complex OS in an automotive head unit.
The co-ax cable that automotive suppliers are working with is the low-cost 3-mm type similar to that now used as antenna cable, Klos says, "For the next generation [of automotive data rates] you won't get Ethernet over UTP (unshielded twisted pair) [to work in the automotive environment]... STP (shielded) would be required, but co-ax is more effective and cheaper." You can expect bi-directional operation, Klos adds, and you may see power over the same cable. This, he says, suits users who don't want to use optical media: nevertheless, the MOST organisation expedts attention to return to optical fibre for data rates in the 1 – 5 Gbit/sec range, possibly including glass fibre.
To enable development and speed time to market, Microchip is also announcing the Physical+ Interface Board OS81118. This board encapsulates the entire physical hardware interface of a MOST network. The Physical+ Interface Board OS81118 comes with a USB 2.0 interface supporting optical and coaxial physical layers, and is expected to be available in Q3/2013. The OS81118 occupies a 72-pin QFN package and will be available for volume production in January 2014.
Microchip; www.microchip.com/get/472T

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Multi-channel, multi-standard signals to 6 GHz from R&S vector generator

Rohde & Schwarz has introduced the SMW200A high-end vector signal generator that creates complex multichannel scenarios: primarily for communications product development, it incorporates MIMO and fading requirements. High on the list of achievements that R&S claims for the new instrument are the ability to generate a variety of MIMO signal patterns, with fading on all paths.

The MW200A high-end vector signal generator creates complex, digitally modulated signals of high quality, with a range of applications that extends from single-path vector signal generator to multichannel MIMO receiver tester.

It combines a baseband generator, RF generator and MIMO fading simulator in a single instrument: it can also manage further connected sources as if they were part of the single instrument. The generator covers the frequency range from 100 kHz to 3 GHz or 6 GHz and has an I/Q modulation bandwidth of 160 MHz with internal baseband. Its modulation and RF characteristics suit it to developing high-end components, modules and complete products for wideband communications systems such as LTE-Advanced and WLAN IEEE 802.11ac, and meets the needs of verification of 3G and 4G base stations as well as aerospace and defence applications.

The R&S SMW200A can be equipped with an optional second RF path for frequencies up to 6 GHz and with a maximum of two baseband and four fading simulator modules, giving two full-featured vector signal generators in a single unit. Fading scenarios such as 2x2 MIMO, 8x2 MIMO for TD-LTE and 2x2 MIMO for LTE-Advanced carrier aggregation can be simulated. Until now, R&S says, this has required complex setups consisting of multiple instruments.

More than two RF sources are required for applications such as 3x3 MIMO for WLAN or 4x4 MIMO for LTE-FDD. In addition to the two internal RF paths provided, R&S SGS100A signal generator modules can be connected as additional RF sources and remotely controlled by the SMW200A. This solution takes up only five height units for 4x4 MIMO receiver tests and provides correctly encoded baseband signals, realtime channel simulation, AWGN generation and, if required, phase-locked coupling of multiple RF paths.

Options for every important digital communications standard are included, and enabled by key-codes: LTE, LTE-Advanced, 3GPP FDD/HSPA/HSPA+, GSM/EDGE/EDGE Evolution, TD-SCDMA, CDMA2000/1xEV-DO and WLAN IEEE 802.11a/b/g/n/ac. The standards run directly , without having to connect an external PC, making it possible to vary signals or specific parameters quickly and easily. This simplifies troubleshooting on the DUT and also saves time. Because the R&S SMW200A is multichannel-compatible, developers can create scenarios using different signals with minimal effort, for example, in order to test multistandard radio base stations. An R&S spokesman cited this as one of the key differentiating factors that makes the stand-alone instrument – as opposed to the modular, PXI-style – format the optimal choice for this class of test unit. The ease-of-control aspect is shown by the fact that a complete test setup of the SMW200A is memorised by a single command.

High accuracy in spectral and modulation measurements comes from SSB phase noise of –139 dBc (typical) at 1 GHz (20 kHz offset). In modulation quality, EVM is –49 dB (measured) for WLAN IEEE 802.11ac signals; as well as a 0.05 dB (measured) I/Q modulation frequency response over 160 MHz bandwidth. ACLR figures for 3GPP measurements (TM1, 64DPCH) are 73 dB at 5 MHz offset and 75 dB at 10 MHz offset.

A touchscreen allows users to control the instrument intuitively with the Rohde & Schwarz block diagram as key operating element to visualise the signal flow. Touching any parameter opens a keypad to set a value: dragging a connection between two functional blocks (for instance, to apply modulation) creates the connection and sets all relevant parameters.

Help functions are provided at all points: presets are provided for all important digital standards and fading scenarios. LTE and UMTS test case wizards simplify complex base station conformance testing in line with the 3GPP specification.

The back panel of the instrument is a module-frame that accepts additional baseband units without requiring calibration of the instrument. R&S comments that one of the achievements of the instrument is to provide in a single box, all of the complex signals, with fading, that previously required a stack of units; compared to the stack that would have been required, the 200A is “half the size, weight and power”, the company says.

The R&S SMW200A can control two further signal sources for complex MIMO pattern generation.

Rohde & Schwarz,
www.rohde-schwarz.com
A video is at; www.rohde-schwarz.com/campaigns/en/smw/video.html

Single-chip digital radio receivers for consumer electronics

Around 1995, says James Stansberry, VP and General Manager of Broadcast Products at Silicon Labs, CMOS processes achieved an fT (transition frequency) of 25 GHz and this, combined with the development of on-chip passives and the ADC technology to directly digitise RF/IF frequencies, set the scene for CMOS RF ICs of the current generation. Much work since that time has focussed on maximising CMOS' strengths and learning to work around its weaknesses; using digital logic to detect and correct RF and baseband performance deficiencies. You can design for cost, without compromising power or performance, he asserts, using DSP to improve selectivity, give channel equalisation, filtering for noise reduction, and using both digital and analogue techniques. The outcome can be single-chip receivers that represent a massive reduction in component count, size, power and cost over a conventional approach.

Stansberry made these observations in the course of introducing Silabs' Si468xFM digital radio IC, that uses software-defined radio techniques for both DAB/DAB+ and HD Radio for portable and home audio products. Claimed to be the first single-die antenna-input-to-audio-output digital radio receiver solution developed for the global portable and consumer electronics markets and using SDR technology, the monolithic Si468x receiver ICs brings FM, HD Radio and DAB/DAB+ broadcast capabilities to a wide range of audio applications, from price-sensitive clock and tabletop radios to high-end multimedia devices with displays, such as mobile phones, tablets and personal navigation devices.

Stansberry believes that digital radio adoption has been slow, in part due to the high cost of delivering a high-performance yet power-efficient RF solution for the consumer electronics market. The Si468x family provides a single-die solution that reduces system complexity, bill of materials (BOM) count and power consumption without compromising RF performance. Using the company's low-IF digital receiver architecture, the Si468x family claims superior RF performance compared to existing consumer-grade digital radio solutions. The receivers support auto-calibrated digital tuning and FM-seek functionality based on multiple signal quality and band parameters and provide flexible audio processing features including noise blanking, configurable FM soft mute, FM de-emphasis and FM hi-cut filtering. It integrates RF tuner, and baseband and stereo audio DACs. Wafer-level chip-scale packaging (WLCSP) supports very compact designs, enabling a complete digital radio receiver system with only 12 external components to be implemented in less than 100 square millimeters.

Receivers are engineered with small form factor designs in mind. By integrating the RF tuner and baseband functions on a single die, the Si468x family avoids radio self-interference and streamlines system design, validation and testing. Silabs claims the smallest footprint and lowest power consumption of any digital radio solution at less than 60 mW in analogue FM mode and less than 95 mW in HD Radio and DAB/DAB+ modes. Si468x receivers support worldwide analogue FM radio reception and incorporate an integrated decoder for the European Radio Data System (RDS) and North American Radio Broadcast Data System (RBDS) standards including required symbol decoding, block synchronisation, error detection and error correction functions. The Si468x family includes the first truly monolithic digital radio receiver ICs certified by

Worldwide FM and digital broadcast radio reception can be added to a variety of products with low BoM cost.

iBiquity to support the HD Radio standard for portable and consumer electronics applications. The Si468x receiver family is compatible with the European Eureka 147 DAB and DAB+ standards and is designed to be fully compliant with the United Kingdom's Minimum Specifications for DAB and DAB+ Personal and Domestic Digital Radio Receivers. Si468x digital radio receivers come in two package options: a 7 x 7 mm 48-pin QFN package and a 3.2 x 3.8 mm WLCSP package. Pricing begins at $5.62 (10,000). An evaluation kit is priced at $550.00.

Silicon Labs;
www.silabs.com/FMtuners

Battery monitoring technology adds precision for lead-acid chemistry

Texas Instruments has introduced a "gas gauge" IC with an "Impedance Track" function that accurately monitors state-of-health, and state-of-charge of lead-acid batteries used in uninterruptible power supplies and e-bike designs. The first lead-acid battery management gas gauge integrated circuit with TI's proprietary Impedance Track capacity measurement technology, the bq34z110, which comes in a 14-pin package, is the only scalable power management device to support multi-cell lead-acid battery packs with battery voltages of 4V, 12V, 24V, 48V and higher. Lead-acid batteries typically behave better than lithium chemistries in environments with wide temperature ranges. However, today's lead-acid battery designs do not accurately measure and report current battery capacity, which often frustrates the end user, and could mean adding more batteries to keep the system adequately charged. The bq34z110 gauge with Impedance Track technology constantly informs a user about the battery's state-of-health and state-of-charge and maintains up to a 95%-accurate capacity measurement for the entire life of the battery. This information also prevents premature shutdown, increasing the longevity of the battery and end-equipment. The bq34z110 is a multi-cell scalable battery gauge to support a wide range of lead acid batteries (4V to 64V), including large capacity batteries (1 Ahr to 65 Ahr and higher) and high-current applications (0A to 32A and higher). Impedance Track uses current, voltage measurements, temperature and battery characteristics to determine battery state-of-charge, state-of-health and capacity. The chip is supported with application notes, user guide and bq34z110EVM evaluation module.

TI, www.ti.com/bq34z110-pr-eu

BY HOWARD JOHNSON, PHD

MEASURING NOTHING

Every scope probe picks up extraneous noise. Some of that noise is self-generated, and some may be generated by the system under test. When looking at a noisy, jittery signal, how can you tell which parts of the signal are "real" and which parts derive from noise and interference? There is only one way, and that way, if you embrace it, leads to remarkable insights about noise, grounding, and the nature of digital systems.

The only way to directly observe noise and interference is to attempt to measure nothing. With your probe in place, grounded as it will be for the actual signal measurement, touch the tip of the probe to any nearby point of ground. This configuration is called a null experiment. Ideally, you should see zero, zip, nada, or, as the English call it, "naught." What you actually observe is your own noise floor, a plethora of noise sources, a whole ecosystem of interferences all superimposed. Creative use of your trigger circuits combined with vertical averaging can often pull apart these tiny effects, deeply buried in a sea of foam, for close inspection. You can learn a great deal measuring nothing.

In theory, whatever noise the probe picks up in your null experiment will appear as noise superimposed onto your actual signal, provided the probe is held in a similar physical position. Two main things cause the noise you will see: one, currents flowing on the probe shield due to differences between the electrical potential of the digital logic ground and the scope, and two, interactions between the electromagnetic fields surrounding the device under test and the probe or probe wiring.

To determine how much noise the former source creates, keep the probe connected to its own ground, but disconnect the probe and probe ground entirely from the device under test. Keep the probe topology otherwise similar to the null experiment. This procedure eliminates the probe-shield currents, leaving only the electromagnetic pickup.

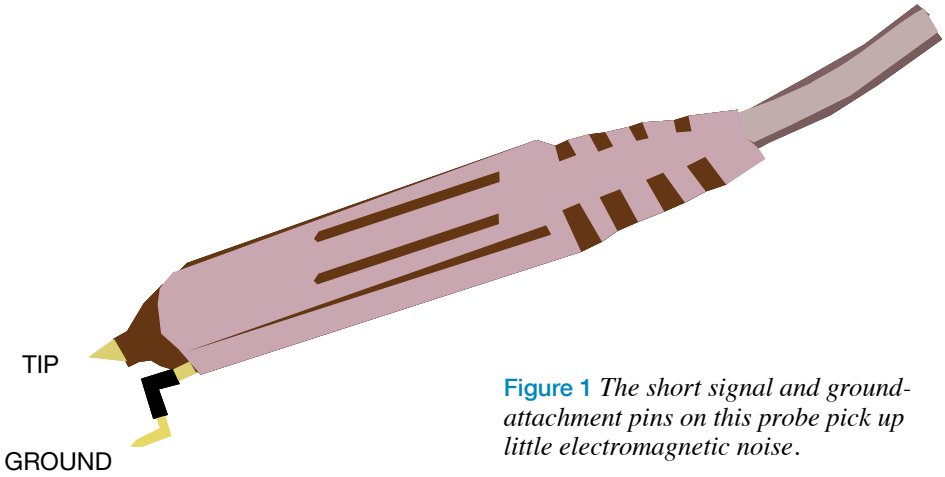

Figure 1 *The short signal and ground-attachment pins on this probe pick up little electromagnetic noise.*

If probe-shield currents are a serious problem, try a differential probe, with one leg on the signal and the other on digital logic ground. Since both inputs to a differential probe have high impedances—much higher than the impedance of a single-ended probe's ground connection—little shield current will flow during this configuration.

Every probe picks up extraneous noise.

Regarding the latter source, first determine if the noise is coming from the device under test or something else in the room. With the probe connected to its own ground, but still disconnected from the device under test, pick up the probe and wave it around. Use the probe as a magnetic-field sniffer to locate the culprit. Sometimes a fluorescent light or other circuit may induce noise in this configuration. If so, turn it off.

If electromagnetic noise seems to be coming from the device under test, check the length of the ground attachment between the scope probe and the system. The smaller you make the loop from the signal source, to the probe, and back through the probe's ground connection, the less noise your probe receives (Figure 1). Reduce the size of that loop, and your null-experiment results should improve.

Understanding why this, and a hundred other tricks, works for noise abatement is all part of the art of digital design. If you want to master that art, follow my advice: "Measure not the thing you know; measure naught."**EDN**

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UMANATH R KAMATH, CYPRESS SEMICONDUCTOR CORP

A SYSTEM-ON-CHIP APPROACH TO INTERFACING STRAIN-GAUGE BASED SENSORS

Strain gauges are useful sensors to measure the mechanical strain within an object. They are attached using adhesives to the object which is experiencing a force. The resulting change in electrical resistance of the strain gauge element contains information about the applied force. The technique has varied applications of which the most common is weighing scale design, and which include force measurement in various mechanical devices, for example pneumatic valves and civil engineering applications, impact sensors, medical sensors, to name only a few.

With so many applications, strain gauges are useful industrial sensor components. In order to make an accurate measurement of the force applied, understanding the strain gauge and its parameters is important. The sensor signal (change in resistance) needs to be efficiently conditioned so that the resulting signal-to-noise ratio from the system is sufficient to accurately determine the magnitude of stress. (Stress is the force applied to the mechanical structure, that we wish to infer: strain is the resulting deformation.) The measurement system includes an analogue signal conditioning path followed by conversion to digital code. This article begins with an understanding of a strain gauge and proceeds to the various non-idealities one has to be aware while interfacing them. Finally an example of system design for read-out of such sensors is shown using a programmable system-on-chip approach: analogue integration is a practical approach which improves the overall realisation of such an interface circuit for strain gauges.

UNDERSTANDING A STRAIN-GAUGE

Strain is defined as deformation (within elastic limits) of a body under the application of force. It is a dimensionless quantity and can either be tensile or compressive depending on the surface to which the strain gauge attached.

When a body is under application of a uniaxial force, there is an extension in its length along same direction, as shown in Figure 1. While elongating, it also experiences a perpendicular contraction. This is defined by the Poisson ratio, which is the negative ratio of strain in the perpendicular direction to the strain in the axial direction. Typically a strain gauge has a serpentine/ wound pattern in order to maximise the area of the conducting material that comes under the influence of the applied force.

Figure 1. *Concept of Strain*

The strain gauge is bonded to the object which is directly exposed to the force. This is known as carrier and transfers the change in physical quantity into a linear change in electrical resistance of the strain gauge. Gauge Factor(G) is used to relate this transformation and is given by:

$$G = \frac{\Delta R / R}{\Delta L / L} = \frac{\Delta R / R}{\varepsilon}$$

The strain-gauge has a nominal resistance which is usually between few tens of Ω to few kΩ. The first challenge in interfacing the strain-gauge to the electronics is the magnitude of the resistance change. For example, a maximum value of 1m strain together with a gauge factor of 2 gives a resistance change of only 0.2%. This change is very small when we consider the nominal resistance. The typical change can be few Ω or much lower. In addition to dealing with such low resistance, there can be many sources of errors during the transfer of force to the resistance change. Ideally the force applied should have a (linear) proportional increase in the resistance. But this is not the case due to the parasitics, for example lead wires from the strain gauge to the circuit can have a larger resistance than the actual change. Also, temperature co-efficients of the strain-gauge resistance can be crucial as the measurement becomes dependent on another factor. In order to correct for these factors, manufacturers usually compensate for the gauge depending on the temperature co-efficient of the material to which it is attached. This reduces the thermal sensitivity but does not completely eliminate it.

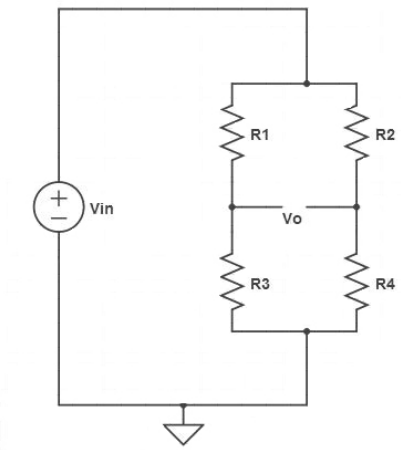

Figure 2. *Bridge method to readout resistive sensors*

RESISTIVE SENSOR READOUT

A common method to readout the sensor information is by Wheatstone bridge configuration (Figure 2), in which the imbalance caused by changes in the sensor resistance results in a voltage difference.

The information from the strain gauge is contained in the differential signal (Vo).

$$V_o = \left(\frac{R_4}{R_4 + R_2} - \frac{R_3}{R_3 + R_1} \right) V_{in} \quad (1)$$

One of the simplest measurement methods is to have one resistance of the bridge (R1) replaced by the strain gauge while other resistance of the arm is kept constant, at the nominal resistance of the strain gauge (R3=Rn). This is called the quarter bridge method. R2 and R4 are held at the same magnitude resistance.

$$R_1 = R_n(1 + \varepsilon G)\Omega \quad (2)$$

Using the above assumptions in (1) gives us:

$$V_o = \frac{\varepsilon G}{4} \left(\frac{1}{1 + \frac{\varepsilon G}{2}} \right) V_{in} \quad (3)$$

One additional modification to the quarter-bridge circuit is to add a very accurate shunt resistance across the bridge, which can be used to calibrate the arrangement. (Finding the voltage difference with shunt resistance, and without shunt resistance, will give a measure of voltage change per Ω change).

As seen from equation 3, the output voltage depends on a non-linear term. In order to remove this, we can modify the bridge to include – instead of R3 – a dummy strain gauge perpendicular to the applied force. This gauge is affected by temperature in same way as the measuring element but is not affected by the sensing quantity.

Going one step forward, we can have an active gauge which is affected in the opposite direction (compress as against elongate), thus making the output linearly dependent with twice the sensitivity as given by equation 4. This is known as half-bridge method.

$$V_o = \frac{G\varepsilon}{2} \quad (4)$$

An extension of the same principle is including active elements in each resistance, with each arm having gauges affected by increase and decrease of the applied force. This is also known as the full-bridge method, and involves using four strain gauges and results in the most sensitive response in terms of magnitude.

$$V_o = G\varepsilon \quad (5)$$

When using a full bridge, maximising circuit sensitivity is achieved by including two gauges in transverse direction with two in the axial direction of measurement of force. It should be noted that using four bridges does not increase circuit sensitivity. Therefore it is not economical to use four gauges; instead two gauges should be connected in series for one quarter of bridge.

SOURCES OF ERROR

Firstly in all the previous analysis, we assumed ideal components. In real-world applications, tolerances on the resistances come into effect. These result in saturation of voltage as well as a large common-mode offset since the actual resistance change in the bridge is small. Techniques such as offset-cancellation using auto-zeroing or modification to include a balancing circuit to adjust for the tolerances by means of trimming or calibration can overcome this problem.

The second error is due to the wire resistance which connects the gauge to the bridge, which desensitises the strain gauge measurements. As seen in equation 6, this results in a modified gauge factor which should be used for correction when calculating the effective force applied. This additional resistance causes offset and gain errors: dependence of lead-wire resistance on temperature is an additional source of error.

$$\frac{\Delta R_1}{R_1} = \frac{\Delta R_g}{R_g + 2R_L} = \frac{\varepsilon G}{1 + 2\frac{R_L}{R_g}} = \varepsilon G^* \quad (6)$$

The bridge is strapped on to the surface of the object to monitor the applied force. The lead wire introduces additional resistance as well as acting as source of noise pick-up. Including these in a quarter bridge-configurations gives us the output voltage as:

$$V_o = \frac{1}{2} A \left(\frac{1}{1 + \frac{1}{A}} \right) \quad (7)$$

Where factor A is given by

$$A = \frac{\varepsilon G}{2} + \frac{R_L}{R_n} \quad (8)$$

The lead-wire resistance is overcome by using a three-wire connection. Consider the three wire bridge circuit shown in Figure 3. RL indicates the wire resistance while supply (VS) is the excitation voltage to the bridge. Considering R1, R3 to be equal

$$R_G = \frac{R_2(V_S - 2V_O) - 4V_O R_L}{V_S + 2V_O}$$

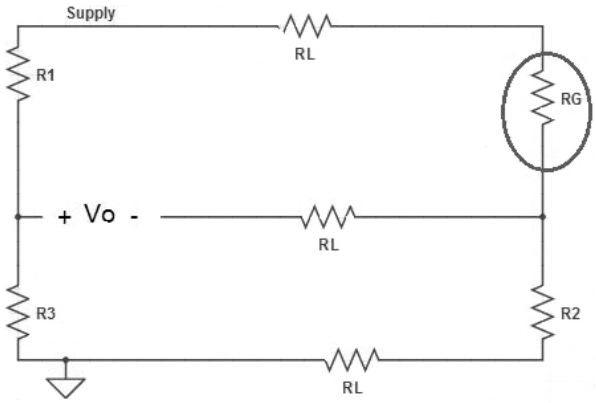

Figure 3: *Three wire connection to the strain-gauge*

The middle resistance through which no current flows, acts as a sense lead. The assumption in order to have complete compensation is that the lead resistances are the same, have the same temperature coefficients and are maintained at same temperature. In reality this is not true and hence other complex schemes such as four-wire or offset compensation mechanisms are used.

INTERFACE CIRCUIT DESIGN

In this section, we discuss a possible interface circuit for strain-gauge; in this implementation, the complete design apart from the bridge itself can be encapsulated in one of Cypress' Programmable System-on-Chip (PSoC 3) devices. The overall design is shown in Figure 4. The configuration we use here is a modulation scheme in which a sinusoidal signal is used.

The PWM generator is used to feed the source excitation signal through a bandpass filter with centre frequency of 5 kHz, to the bridge. An active bandpass filter is realised using the available opamps within the PSoC. The components identified as C_hpf and R_hpf control the high-pass filter response while R_gain and R_gainf provide the gain, and where R_lpf and C_lpf provide the low-pass filtering. A cascade of these configurations provide the required bandpass behaviour which filters the sinusoid from the PWM generator, to be fed to the bridge as excitation source. The signal is then amplified by the instrumentation amplifier, which uses the three-opamp topology, before being down-converted using the mixer and the same sinusoidal signal source. The down-converted signal which contains the sensor information (difference in node voltages) is digitised by a ΣΔ converter. The ΣΔ converter can have up to 20-bits of resolution based on the sample rate required from the read-out channel.

The strain gauge is a useful sensor in industrial applications, given that its principle of operation is understood and its various forms of errors are taken into account. This article has shown a method of interface circuitry using carrier frequency excitation of the bridge. The complete design can be implemented on-chip using Cypress' PSoC which increases the performance and provides the required accuracy in such interface applications.

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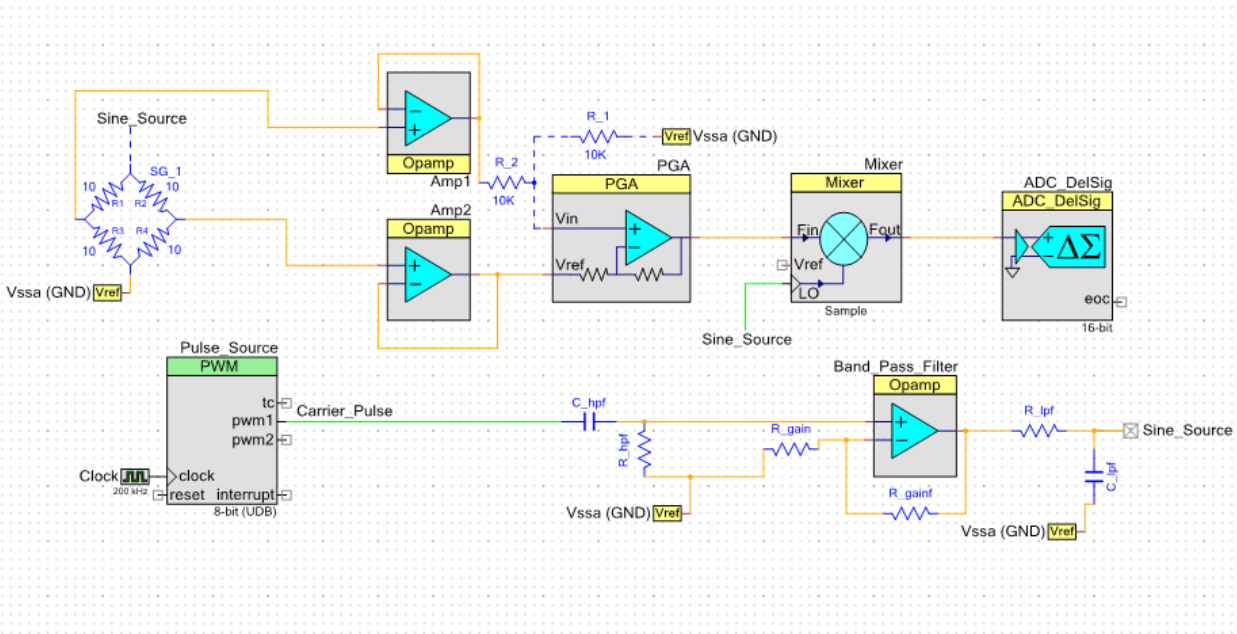
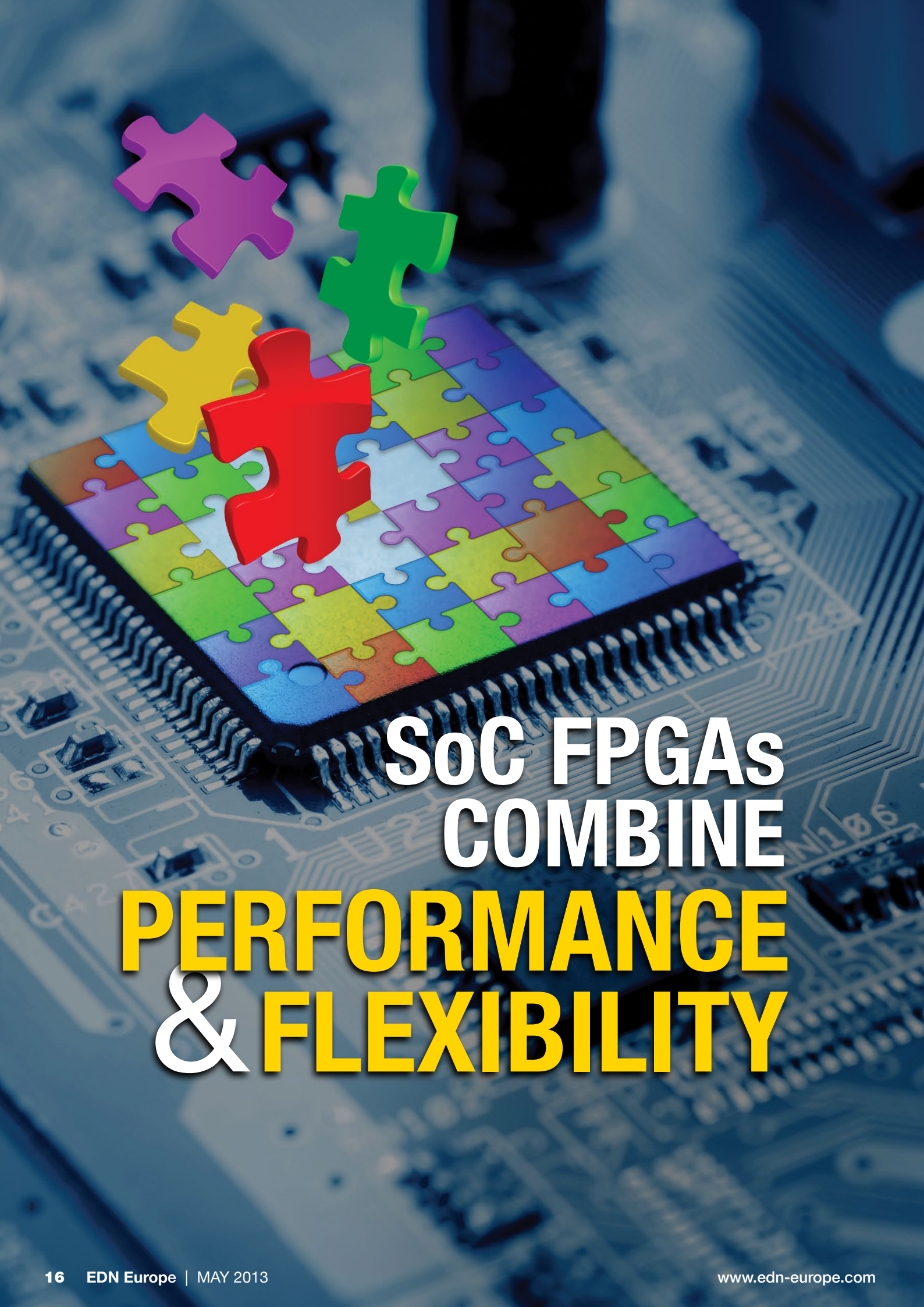


Figure 4. *Example of an interface circuit for strain-gauge sensor using Programmable System-on-Chip*



SoC FPGAs COMBINE PERFORMANCE & FLEXIBILITY

EMBEDDED-SYSTEM ARCHITECTURES BUILT ON A COMBINATION OF MCUS AND FPGAS OFFER THE KIND OF ADAPTABILITY INCREASINGLY REQUIRED TO SUPPORT CHANGING DEMAND FOR GREATER FUNCTIONALITY ACROSS DIVERSE APPLICATIONS.

BY MICHAEL PARKER • ALTERA CORP

With the integration of dual ARM A9 CPU cores, a complete set of ARM peripherals, the ability to implement in hardware either fixed or floating-point signal processing, and unmatched I/O flexibility, the latest FPGA system-on-chip devices can perform what used to require a complete circuit card containing dozens of chips. A perfect example is next-generation motor control.

Next-generation motor-control systems are designed to deliver maximum motor efficiency using very fast control loops that exceed the capabilities of processor-only solutions. The inner control loops, implementing what is known as field-oriented control (FOC), require transforms best performed in floating point. FPGA SoCs that combine dual processor cores and FPGA fabric are ideal for this application, combining in a single device the capabilities of general-purpose processors and high-performance logic for specialized algorithms (see sidebar “How FPGAs and multicore CPUs are changing embedded design”).

MOTOR COMMUTATION

Electric motors rely on basic electromagnetic principles. Forces due to magnetic attraction and repulsion are used to generate torque, as well as the resulting rotary motion of the motor.

Magnetic fields are generated in both the rotor and the stator, through the use of either permanent magnets or electromagnets. Proper alignment of the magnetic fields as the rotor turns is required.

The magnetic fields must continuously change to maintain an alignment that produces torque throughout the rotor's full 360 degrees of rotation. This process is called commutation. The most basic method used is the dc brush motor. This motor design has permanent magnets in the stator and one or more electromagnet pairs in the rotor. In order to eliminate the sparking and wear of brushes for mechanical commutation, the motor design can be turned inside out by placing the permanent magnets on the rotor, and the electromagnets in the stator. Replacing mechanical with electronic commutation can achieve the same effect, and is known as a brushless dc motor.

FIELD-ORIENTED CONTROL

In a dc brush motor, the control loops can simply drive the motor current variable, and the brushes perform the mechanical commutation function, although in a suboptimal fashion. With FOC, sinusoidal commutation will be performed electronically in an optimal fashion, using integrated control loops to maximize the magnetic field components producing useful torque and minimize magnetic field components that do not yield torque (perhaps, for example, merely exerting force on the motor bearings). The object of FOC is to ensure the magnetic fields are precisely orientated at all times to produce maximum torque, eliminate torque ripple, and thereby increase motor efficiency and lower the cost of ownership of the system.

The FOC function shown in **Figure 1** uses Park and Clarke transforms as well as PI control loops for torque (useful oriented magnetic field direction) and flux (magnetic field direction producing no torque). PI controllers are used rather than the PID controllers typically seen in control systems. (The derivative term is not used.)

Motors normally use three independent phases. These phases can be replicated around the stator, giving the number of poles or windings. In a three-phase system, the sum of the currents is defined as zero by Kirchhoff's law.

AT A GLANCE

- Given the rapid growth of new standards and protocols as well as increasing pressure to speed time to market, embedded-system design is due for a disruptive paradigm change.
- The latest FPGA system-on-chip devices can perform what used to require a complete circuit card containing dozens of chips.
- SoC FPGAs for real-time applications such as motor control provide both integration benefits and the ability to scale performance.

This means that a three-phase current vector (a, b, and c components) can be expressed as two orthogonal phases (α, β components), using the Clarke transform. The Clarke transform is valid at a given rotation angle of the rotor.

Using the Park transform, these current vectors are mapped onto the rotating plane of the spinning motor. This results in the α, β components being mapped into q (quadrature) and d (direct) components. The transform requires the rotor angle, which is the input, often determined by a quadrature encoder attached to the rotor shaft. The Clarke and Park transforms, therefore, need to be continuously calculated as the motor rotates.

REQUIREMENTS

While motor-control applications are mechanical, the rate at which the drive circuits must be updated and the current, position, and speed sensors read can be quite high. A reasonable scenario might be a motor operating at a maximum of 12,000 RPM, or 200 revolutions per second (RPS). If we use a rule of thumb that a minimum of 80 samples is needed to generate a well-shaped sinusoidal current waveform, then the required sample rate will be the equal to motor speed (RPS) × 80 × number of motor pole pairs.

The number of motor pole pairs is the number of electromagnetic windings in the stator. For a motor at 12,000 RPM with eight windings or pole pairs, this works out to a sampling rate of 128,000 per second, and a processing latency of

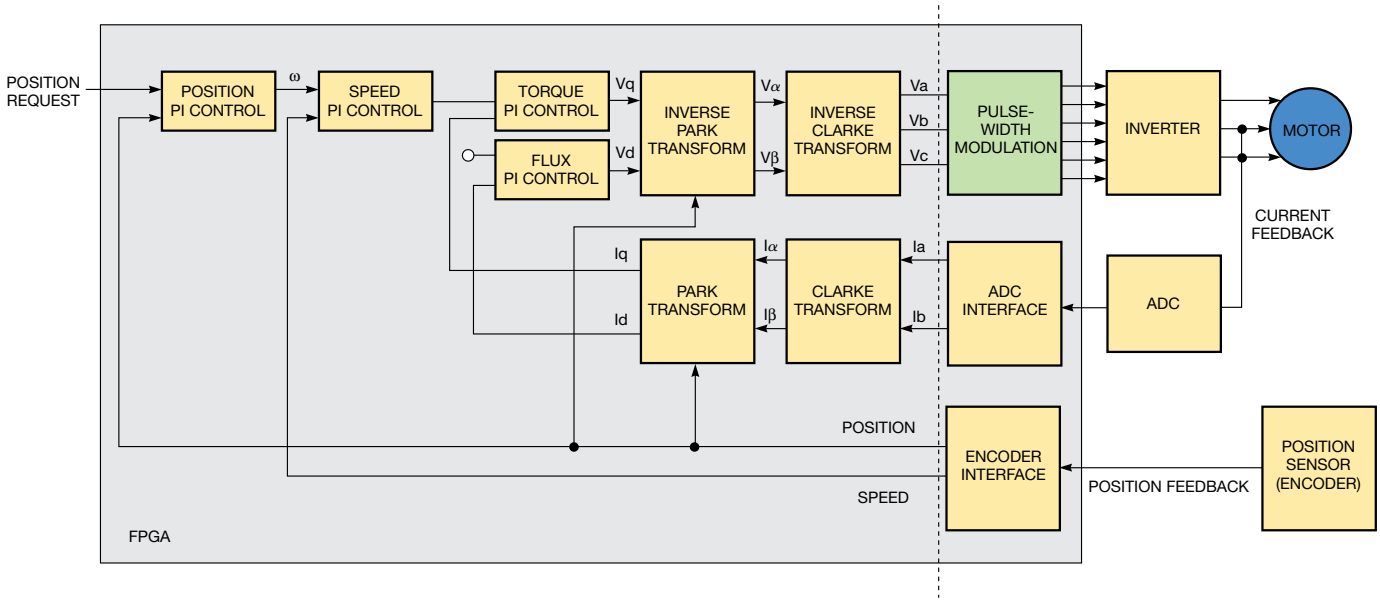


Figure 1 *This FOC-based motor-control system uses Park and Clarke transforms as well as PI control loops for torque and flux.*

HOW FPGAs AND MULTICORE CPUs ARE CHANGING EMBEDDED DESIGN

BY SANJAY CHALLA, NATIONAL INSTRUMENTS

With the explosion of embedded devices in the past few decades, many improvements have been made in both the hardware components and software tools. Despite this innovation and growth, however, traditional embedded-system design approaches have evolved little if at all and are increasingly proving to be a hurdle. Given the increasingly rapid growth of new standards and protocols as well as increasing pressure on design teams to deliver to market more quickly, embedded-system design is due for a disruptive paradigm change.

With the accelerating growth of advances in hardware technologies and software tools, the challenge posed by integration is set to rise. This challenge, if unaddressed, will result in more expensive end products and can prevent experimentation, growth, and delivery of more innovative designs to the marketplace.

STANDARD EMBEDDED ARCHITECTURE

In the general computing marketplace, standardization has resulted in more robust operating systems, more refined end applications, and advances in the underlying hardware components. The lesson learned is that time saved in avoiding the integration effort of custom hardware architectures and associated software components results in better end solutions, which are delivered to market faster.

For the embedded space, a corresponding standard architecture needs to be flexible enough to adapt to diverse use cases while providing an avenue for updates. Given these constraints, the most robust architecture for standardization in the embedded design space is a microprocessor and an FPGA working alongside each other as a single unit (Figure A). Together, these two elements enable substantial flexibility in designs.

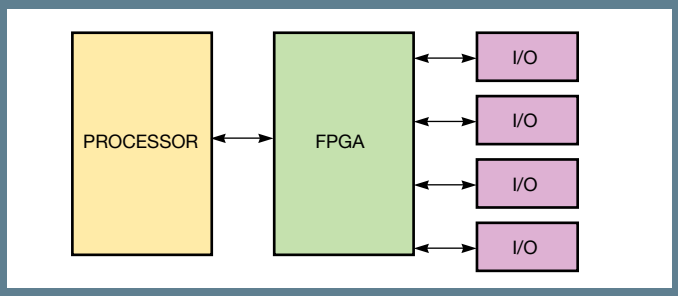


Figure A *In this standard hardware architecture, the combination of a processor and an FPGA enables flexibility while making it possible for standardization that can utilize higher-level tools to make substantial gains in the design workflow. The processor makes it possible to reuse existing code libraries, while the FPGA allows for the flexible implementation of custom algorithms.*

FPGAs offer the benefits of hardware determinism and reliability without the up-front cost and rigidity of ASIC design. Additionally, the ability to load new logic and redefine the connections in the FPGA fabric makes it possible for designers to future-proof designs and benefit from more robust updates without requiring any substantial modifications to hardware.

The combination of processors and FPGAs in embedded-system design is growing in many industries. Embedded-systems developers are using designs based on several processors and FPGAs. The FPGAs are used to take accurate, high-speed measurements or run time-critical algorithms. Meanwhile, the processors run a real-time operating system to handle lower-frequency control loops or provide Ethernet communication to other distributed nodes and facilitate remote data access, system management, and diagnostics.

HIGHER-LEVEL TOOLS

A key benefit of a standard architecture is that more capable and optimized high-level tools can be developed and used for design. Higher-level tools make it possible for domain experts to be more closely involved in embedded-system design with smaller and more efficient design teams. As a result, more complex products can be pushed to market sooner with smaller design teams.

General-purpose computing provides evidence for the efficiencies that can be gained in application development with higher-level design tools and languages. Unsurprisingly, the embedded marketplace has started to witness the growth of higher-level design tools, including the Xilinx AutoESL C-to-Gates high-level synthesis tool, Mentor Graphics Catapult C Synthesis tool, and NI LabVIEW ultimate system-design software.

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Sanjay Challa is a product manager for embedded software at National Instruments, with a focus on real-time operating systems and FPGA-based embedded systems. He joined the company in 2010. Challa received his bachelor's degree in biomedical engineering from the Georgia Institute of Technology (Atlanta).

7.8 µsec.

Each application will be different, but often the system must be designed such that it can acknowledge and process all interrupts and update the motor drivers within 5 µsec or less. The process is to sample the feedback motor currents, position, and speed, and use FOC to calculate updated motor current driver values at a rate of 200,000 per second with a 5-µsec processing latency. For a processor-based system, this implies an interrupt rate of 200 kHz, which can be a significant challenge for general-purpose processors with caches, operating systems, and non-vectored interrupt controllers.

PROCESSING SYSTEM

Use of an SoC FPGA system can allow a more optimal and flexible implementation. The SoC contains two 800-MHz ARM Cortex A9 microprocessor systems.

The ARM A9 processor is a more general-purpose, high-performance processor, but it is not optimized for demanding real-time applications with guaranteed response times. Real-time performance limitations can be mitigated, however, by taking advantage of the integrated programmable logic of the SoC FPGAs. The programmable logic can be used for PWM drive circuits,

TABLE 1 HARDWARE RESOURCES TO IMPLEMENT IN SOC FPGA (5CSEA2)

FPGA hardware resources and performance	Logic elements	Variable precision DSP blocks	M10K memory blocks	F_{MAX}/processing latency
Floating-point FOC, including Park, Clarke, and PI controllers	7.7K	2	1	120 MHz 1.74 µSEC
Available resources	25K	36	140	
5CSEA2 SoC FPGA (%)	31	5.5	0.7	

versatile interfaces to any ADCs and DACs, position and speed sensor interfaces, safety cut-off circuits, a proprietary network or MAC hardware interface, and more. It can also implement the FOC and control loops with less latency and much faster response time than are possible using processor-only systems. Typical system response time is less than 2 µsec, which is about an order of magnitude faster than most processor-only systems can support.

FOC HARDWARE

A design tool such as DSP Builder from Altera can be used to take a Simulink representation of a design and implement it directly into FPGA logic. DSP Builder also generates floating-point logic, just like the simulation, to provide greater dynamic range and numerical stability than fixed-point implementations allow. The resources used to implement in the smallest SoC FPGA are shown in **Table 1.**

All interfaces to the FOC blocks are memory mapped by Altera's DSP Builder and Qsys tools into the ARM processor system. This allows for software control of the desired torque output, for the gains of the PI loops controlling torque and flux, for monitoring operations, and for other functions.

CONTROL-LOOP HARDWARE

The position and speed control loops may also be implemented in logic, similar to the PI control used in the FOC function. The gain stages of the different PID circuits can be updated using memory-mapped registers to the ARM processor. If needed, this can provide extremely low latency and fast response at the same rate as the commutation function. Sub-5-µsec total response of the control and FOC is easily achievable, which can provide more stability for very-fast-reacting systems. Just as in FOC, these control loops can be implemented in hardware from Simulink models, using DSP Builder to provide floating-point hardware in the FPGA logic.

Another consideration is that multiple axes of motor control can usually be added to the FOC hardware with a small increase in logic size and processing latency. A four-axis motor controller may have 20% higher logic use and minimal latency increase over a single-axis implementation. In a software-based implementation, the latency will scale in a roughly linear fashion.

CONTROL-LOOP SOFTWARE

Motor control loops are most commonly implemented in software using C code. Due to the effect of the FOC's isolating the control loops from the motor commutation, the interrupt rates and latencies of the motor control can be determined by the response of the system, which is normally much slower than the PWM commutation circuits. Simulation and analysis are required to determine the minimum update rates for expected performance and stability; however, an update rate of 10 kHz is normally adequate. In this case, the torque settings to the FOC would be updated at this lower rate (every 100 µsec), based upon feedback and calculation of the current position and speed information.

This SoC approach allows for the hardware to be used for the FOC "inner loop" and the ARM A9 for the motor control "outer loop." The inner loop can guarantee latency under 2 µsec in the FPGA hardware. The ARM can achieve very reasonable processing latency under most conditions and is ideal for outer-loop processing where interrupt latency requirements are much more relaxed, and the consequences of missing an interrupt are not catastrophic.

ARM A9 INTERRUPT LATENCY

The following is based on an analysis by the Altera SoC engineering team of real-time system performance of the ARM processors contained in low-cost SoC FPGAs, specifically interrupt latency. Interrupt response time can vary with system configuration, operating systems, cache configuration, and processing-task load.

The team considered the following scenarios:

- **Stage 1:** Highly constrained system on a single core to establish a benchmark for the lowest latency that can be achieved (To measure the maximum achievable performance, this stage did not use an OS, and the tests are implemented using bare-metal drivers.)
- **Stage 2:** Similar to stage 1, but the tests are implemented using an RTOS (µC/OS-II) and the measurements are repeated over a number of iterations (1024) to get a statistical model of the interrupt latency
- **Stage 3**: Similar to stage 2, with multiple background tasks running on the RTOS alongside interrupt latency measurements (This background task writes data onto the UART port in an infinite loop, and in addition, another background task is performing memcpy in the external

TABLE 2 MEASURED INTERRUPT RESPONSE LATENCY (MSEC)

Cache configuration	Stage 1	Stage 2	Stage 3	Stage 4
Cache disabled	2.53	2.65	2.87	2.89
L2 enabled	0.57	0.54	3.53	1.5
L1 enabled	0.16	0.19	1.29	1.29
L1 and L2 enabled	0.16	0.19	1.28	1.3

TABLE 3 MEASURED FOC LATENCY (µSEC)

Cache configuration	Interrupt response (stage 4)	FOC processing	Total latency
L2 enabled	1.5	3.27	4.77
L1 enabled	1.29	0.83	2.12
L1 and L2 enabled	1.3	0.73	2.03

memory in an infinite loop, which generates AXI read/writes that may require a long time to complete.)

• **Stage 4:** Emulation of a larger system where not all code can fit within the L1 cache (In this case, the critical code is placed in the L2 cache. Since the cache is likely to be large enough to hold the whole of the background processing code, after each interrupt, L1 cache flush is triggered. The objective here is to measure the interrupt latency achievable when using the SoC FPGA with a real-time operating system in a real-world environment where cache flushes play a significant role in system performance.)

Cache (L1 & L2) has the most influence on the interrupt latency **(Table 2).** In a stage 4 situation, with the instruction code locked in L2, the latency is significantly lower than the same system running from external memory. With L1 enabled, it is lower still. The latency will be much worse in the stage 3 and 4 cases, however, due to the background tasks that cause the ISR code to be replaced with other background tasks.

The interrupt response latency needs to be added to the processing time of the FOC **(Table 3).** A basic FOC algorithm was benchmarked, including trigonometric functions, Clarke/Park transforms, PID controller, and inverse Park/Clarke transforms.

Due to the processor performance of the ARM A9, a software-based FOC controller has been shown to be able to meet the 5-µsec requirement. There is little margin, however, and interrupt response times are often the most nondeterministic part of the system. While the results shown are the longest latencies seen under these test conditions, much longer times may occur on occasion, due to the statistical nature of the processing-task load. However, in the case where interrupts are occurring at rates on the order of 10 to 20 kHz, or 50 to 100 µsec, it appears that the ARM Cortex A9 can meet the real-time requirements with extremely high margins, and very low probability of not servicing interrupts in a timely manner. By isolating the ARM interrupts from the much higher-speed FOC commutation requirements, real-time performance is virtually assured under a wide variety of operatin-bobg conditions and processing loads.

The use of SoC FPGAs for real-time applications such as motor control provides not only integration benefits but also the ability to scale performance as needed. This approach allows high-rate, deterministic functions (inner loop) to be implemented in hardware, while lower-rate, more dynamic and complex processing (outer loop) can take place in software, providing the best of both worlds to the system designer.**EDN**

THE USE OF SOC FPGAS FOR REAL-TIME APPLICATIONS SUCH AS MOTOR CONTROL PROVIDES NOT ONLY INTEGRATION BENEFITS BUT ALSO THE ABILITY TO SCALE PERFORMANCE AS NEEDED.

AUTHOR'S BIOGRAPHY

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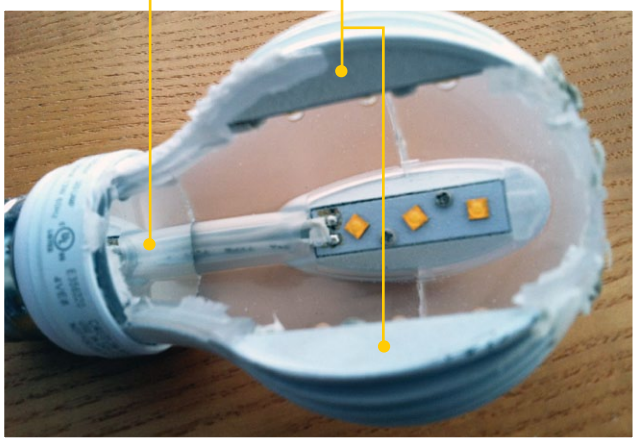
LED light shrinks size, cost with nonisolated driver

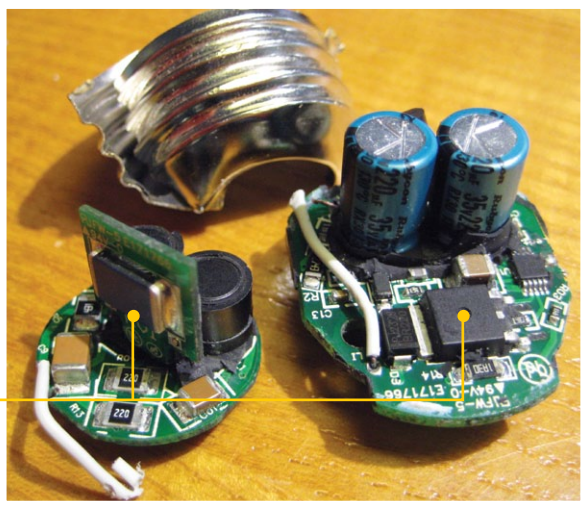
LED-bulb prices are dropping. A year ago you could expect to pay $50 for a Philips dimmable 60W-replacement LED bulb, while today you can go to Best Buy and purchase its house-brand 8W, 800 lumens Insignia 60W-replacement bulb for just $17. What has changed in LED-bulb design to allow this price drop? Tearing apart the bulb gives us a look into some design trends in LED lighting, such as how the LEDs are placed within the bulb and what driver architecture is used.

The Insignia bulb has a shape similar to the familiar incandescent light, with the addition of three metal heat-sink fins and a plastic bulb instead of glass.

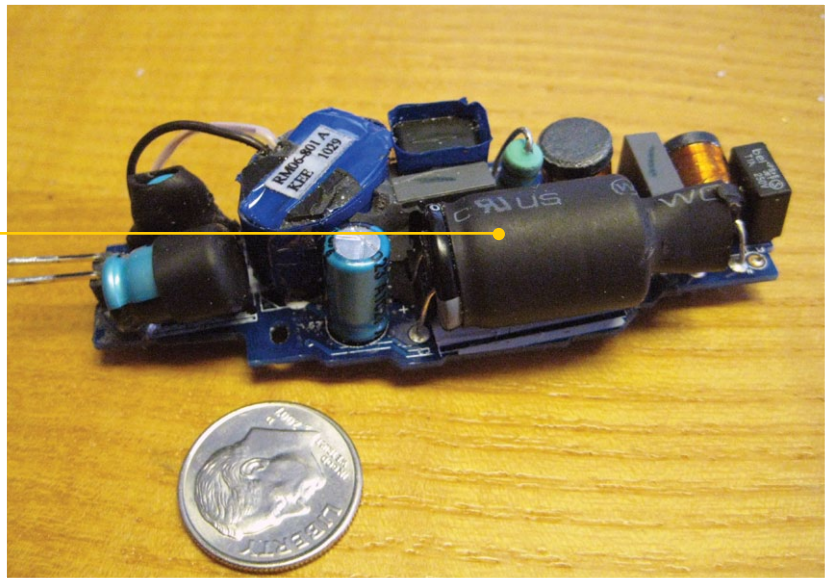
The plastic bulb cover was removed with a Dremel tool, exposing the six Cree white LEDs that illuminate the bulb's light-mixing chamber, which allows an even glow with no pixelation. The metal fins on which the LEDs are mounted serve both to elevate the LEDs and as heat sinks. At the bottom of the mixing chamber is a paper-thin aluminum reflector that helps reflect the light up and out of the bulb. All of the electronics for this bulb lie beneath the mirror in the base of the bulb, in a separate and encapsulated compartment.

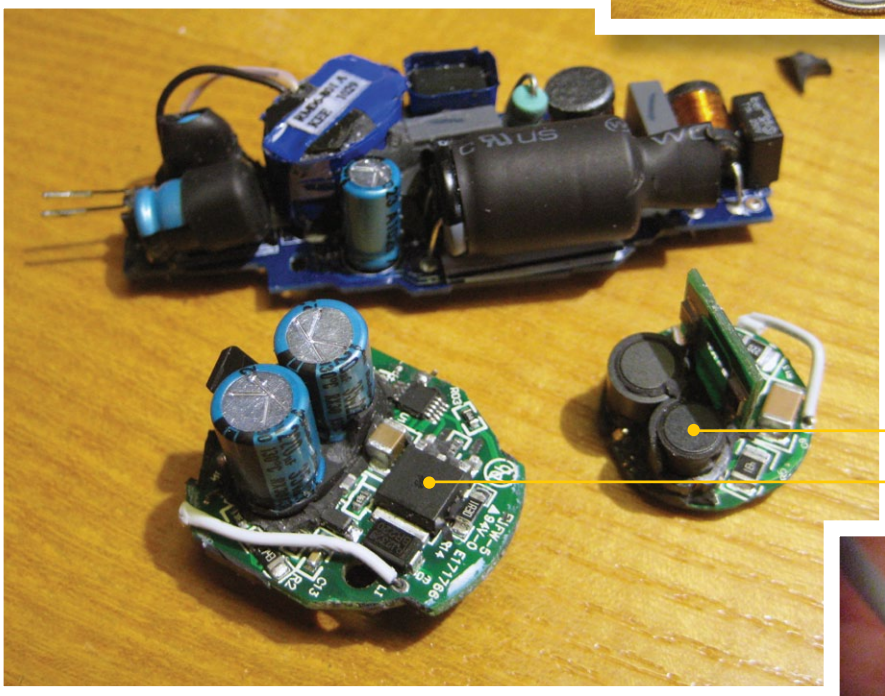


Removing the rubbery potting compound shows that the electronics are mounted on two PCBs that nestle together. Here, the PCBs are separated and next to the bulb's base.

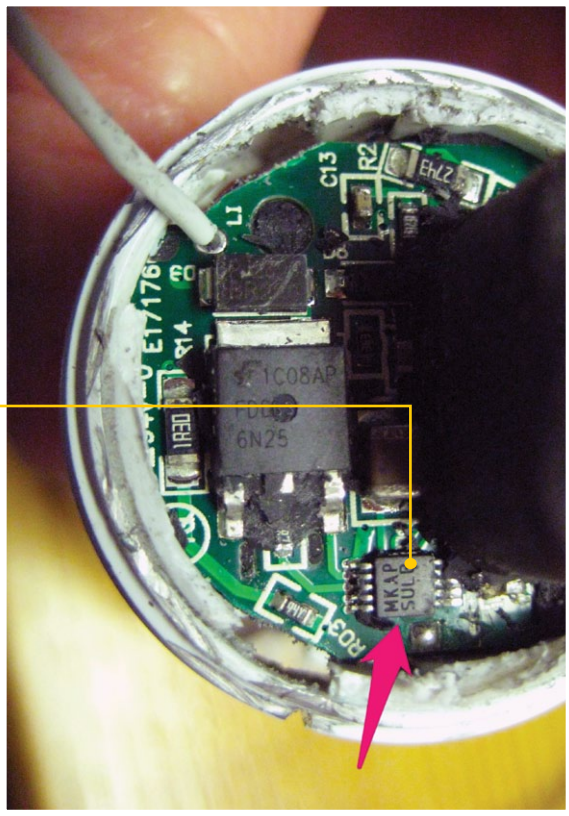


For comparison purposes, the driver electronics are shown for an LED-light teardown from about a year ago. Not only is the packaging quite different, but also there are a lot more electronics. For example, the older design has three electrolytic capacitors and a very large transformer.





The two different generations of drivers are shown side by side: The Insignia driver has just two relatively small e-caps. This setup raises the question: What LED-driver IC does the bulb use, and how does it allow such a tiny driver?



Question answered: The "SUL B" on the tiny IC is the marking for the Texas Instruments LM3445. There is no transformer, indicating that the LED-driver design is nonisolated. The incandescent-bulb design itself is nonisolated. If you broke the glass in an incandescent bulb while it was plugged in, you would have direct access to the ac-line power. Clearly, nonisolated designs can be made fully compliant with UL specifications. Note: While a nonisolated ac/dc LED-driver design can both be safe and meet UL specifications, developing and testing a nonisolated offline LED driver in the lab requires stringent lab-safety procedures.

Dimming is an important bulb characteristic for the US market.

I used a Lutron Maestro dimming switch, with a programmable dimming control, and did a side-by-side comparison with an incandescent bulb. The Insignia dimmed consistently and smoothly, with a dimming profile similar to the incandescent bulb.

Watch a video of the dimming test at http://bit.ly/145ROBK.

THOMAS WENZEL, GOEPEL ELECTRONIC

TEST & MEASUREMENT TECHNOLOGY GOES EMBEDDED

The term “embedded” can be found in nearly every development sector. And everybody is working to broaden the embedded factor, be it on the chip or board level. In particular, the high rate of innovation occurring in microcontrollers and FPGAs enables opportunities for creation of multi-functional electronics, that are more intelligent, more suitable for networking, re-configurable, and compact in size. New 3D chip technologies will boost this trend as the hunger for smart solutions in sectors such as cars, consumer electronics, aerospace, and industrial electronics is insatiable.

Successful development of such highly complex products requires excellent command of software design, FPGA design, and board design. No less important are excellent skills in coordination of all distinct stages of development, from design concept to final prototype validation. In this context the so-called “V-model” plays an important role (see Figure 1).

The V-model defines adequate verification procedures for every design step to ensure a structured final overall validation. Throughout the current model, structured process steps have complemented pure functional considerations. This is due to the fact that structured validation and tests, as elements of a design-for-testability strategy, have become standard in modern design and production test environments, and their importance is still increasing.

To be able to meet the requirements test probing of signals can, today, only partly serve as a developer’s means of accessing the required signal information. Test engineers suffer from the same experience when it comes to the use of traditional in-circuit-test strategies in production. Here miniaturisation in electronics leads to problems: reduced test coverage, tremendously increased costs of fault-finding, and, finally, the feared ‘no-failure-found’ syndrome.

Common suffering, however, sometimes leads to completely different reactions. Some people start to haggle over every test point for every new design, others switch to using using flying probe testers (which are capable of contacting very small areas down to pin lands), and still others look to improved functional tests as the only way forward. However, the reality is that neither in-circuit-tests nor flying probers can really help to solve the validation problem. And test points are disappearing. So, the need for an alternate strategy is really urgent here. But if access is possible, It might be thought that all this discussion should no longer be necessary.

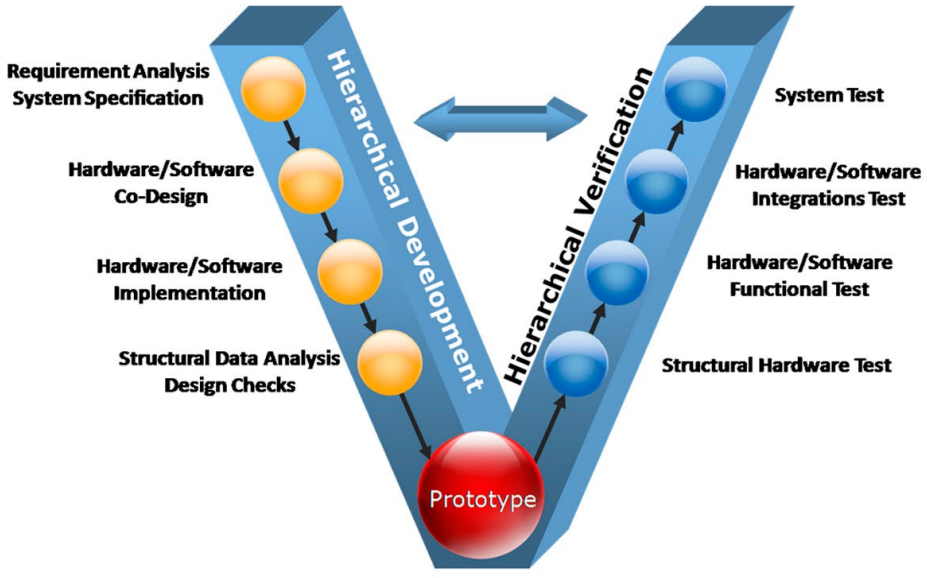


Figure 1 *Definition of hierarchically structured development and verification*

THE ART OF MEANINGFUL SEEING

To transmit and process information faster, you need to increase the speed of internal signal flow. In addition to the transition to parallel processing using multi-core systems, an additional trend is increased signal transmission rate. This is especially important in the changeover to serial Gigabit links. Externally, such Gigabit connections are implemented using standard communication buses such as USB3.0, PCI Express, or SATA Express. For instance, they are increasingly used as a high-speed transmission medium for chip-to-chip communication on board.

One of the top drivers of innovation is FPGA technology. The latest generations of FPGA devices from Xilinx or Altera offer fantastic transmission rates of up to 28 Gbit/sec – in parallel on up to 96 channels. However, the design-in process of such Gigabit links requires great care. Due to the high frequencies involved, these connections are bound up with the typical challenges of analogue technology, though differential transmission technology relieves some of the pressure.

Design rules are extremely stringent and require an impedance-matched implementation to ensure the highest quality of signal transmission. High-quality Gigabit analysers with special test probes are available to validate such connections. Nevertheless, probing of Gigabit signals will always affect signal integrity. It’s like the task of touching a glassy water surface without generating waves; at best, the waves might be

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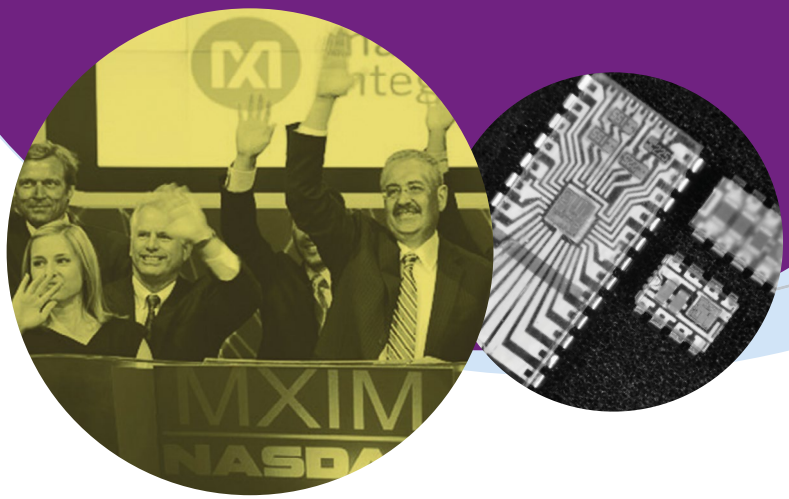

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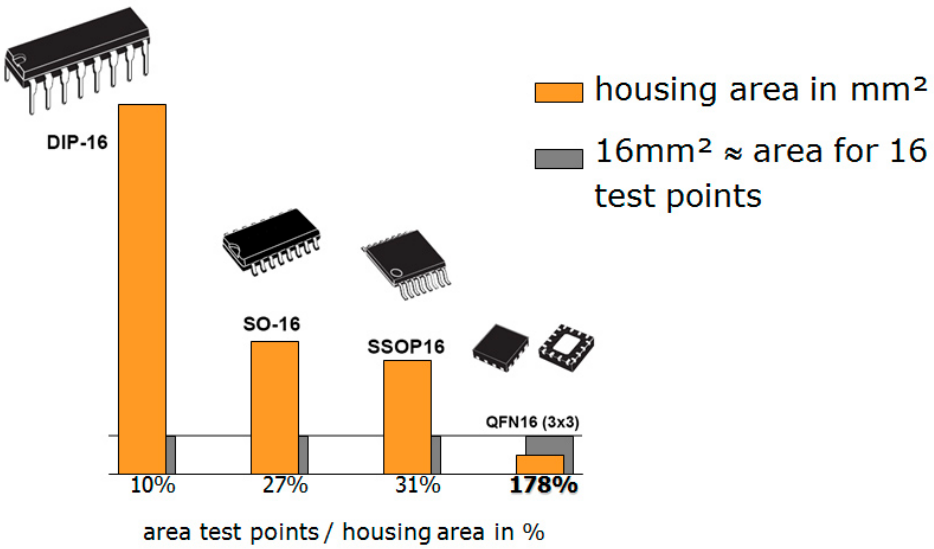

Figure 2 *The required board area for test points is getting more critical*

minimised.

Modern Gigabit analysers try to tackle this problem using some sort of de-emphasis to compensate for probe properties. Real induced anomalies, however, can only be precisely calculated when the interaction of electrical properties of probe and probe target are known – and thus they remain invisible. The transmission frequency is the key figure in this context, and, as it is ever-increasing, anomalies will be increasing too. So external instruments will hit their natural limitation (see Figure 3). Assessing the whole picture from the design's point of view clearly spells out: we don't see what silicon sees. And this becomes increasingly problematic.

EMBEDDED SYSTEM ACCESS (ESA)

Analysis of current access strategies suggests a division into three classes:

- Native Connector Access (test access via design-relevant I/O signals)
- Intrusive Board Access (artificial access via test nails and probes)
- Embedded System Access (natural test access via design-integrated test bus)

In practice, these classes are not isolated but can be applied in combination.

As a result of these challenges, embedded system access [Reference 1] sounds promising. The roots reach back more than twenty years – originating from the boundary scan test method, which was standardized in 1990 as IEEE1149.1 [Reference 2]. Driven by evolutionary developments, ESA today covers a variety of non-intrusive technologies to validate, test, debug and program electronics assemblies. These include, specifically;

- Boundary scan test (IEEE1149.1/4/6/7)
- Processor emulation test (PET)
- Chip embedded instrumentation (IJTAG/IEEEP1687)

The basic idea of ESA is to replace the tactile access with access that is integrated into silicon. In principle, every ESA technology has its task-specific "pin driver" electronics, which are controlled via a test bus to run test functions or programming tasks directly in-system. The target system may be a chip, a board, or an entire unit. Hence, it is totally independent of the hierarchical application level. So the ESA concept can be used throughout the V-model and the entire product life cycle.

T&M GETS SYSTEM-INTEGRATED

The transition to ESA isn't just a small adaptation of how to handle test and programming vectors: it is a paradigm shift. The practical use of ESA implies the conversion of a unit under test's (UUT's) pure functional design into a tester-UUT-configuration (see Figure 5).

The transformation forms a three-level infrastructure. This comprises a test bus (typically JTAG) as control medium, the so-called pin electronics (which provide the internal interface to the target), and the elements of the UUT that need to be validated or tested. The pin electronics are driven by boundary scan, the microprocessor, and chip-embedded instruments. But what, precisely, are chip-embedded instruments and how can they solve the problem of Gigabit links?

INSTRUMENTS THAT SEE THE SILICON

Chip-embedded instruments are test and measurement intellectual property (IP) blocks integrated into ICs, which are controlled via the test bus (see Figure 6). Of course, the IC may have boundary scan included.

Examples of chip-embedded instruments include voltmeter, frequency meter (counter), thermometer, bit-error-rate tester (BERT) for high-speed signals, logic scope, RAM tester, built-in self-test circuitry (BIST), and the in-system programmer.

The IP is either permanently integrated in the chip (hard macro), or it can be temporarily instantiated and configured (soft macro) in FPGAs. As all instruments can be controlled serially or in parallel;

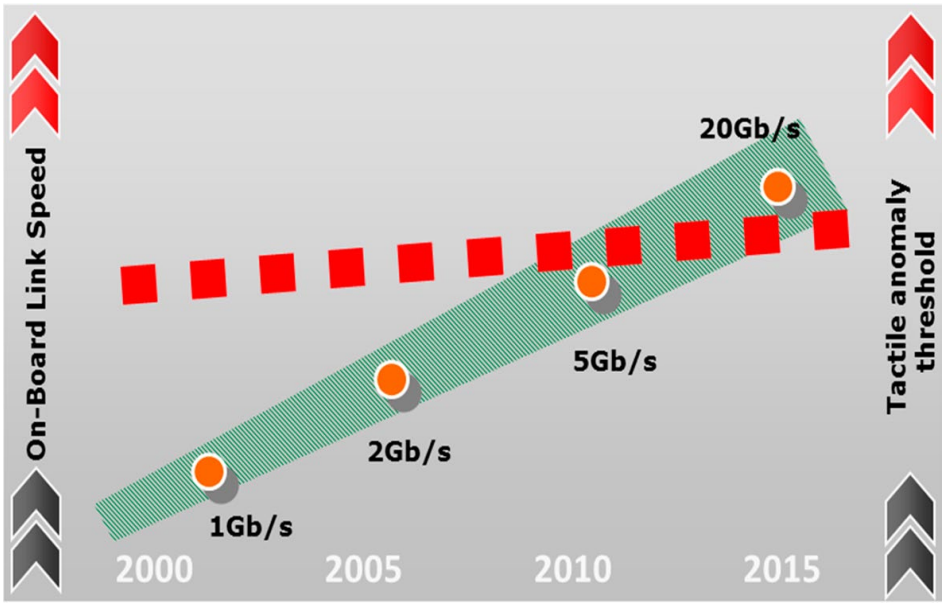

Figure 3 *Probing of Gigabit signals hits a critical limit*

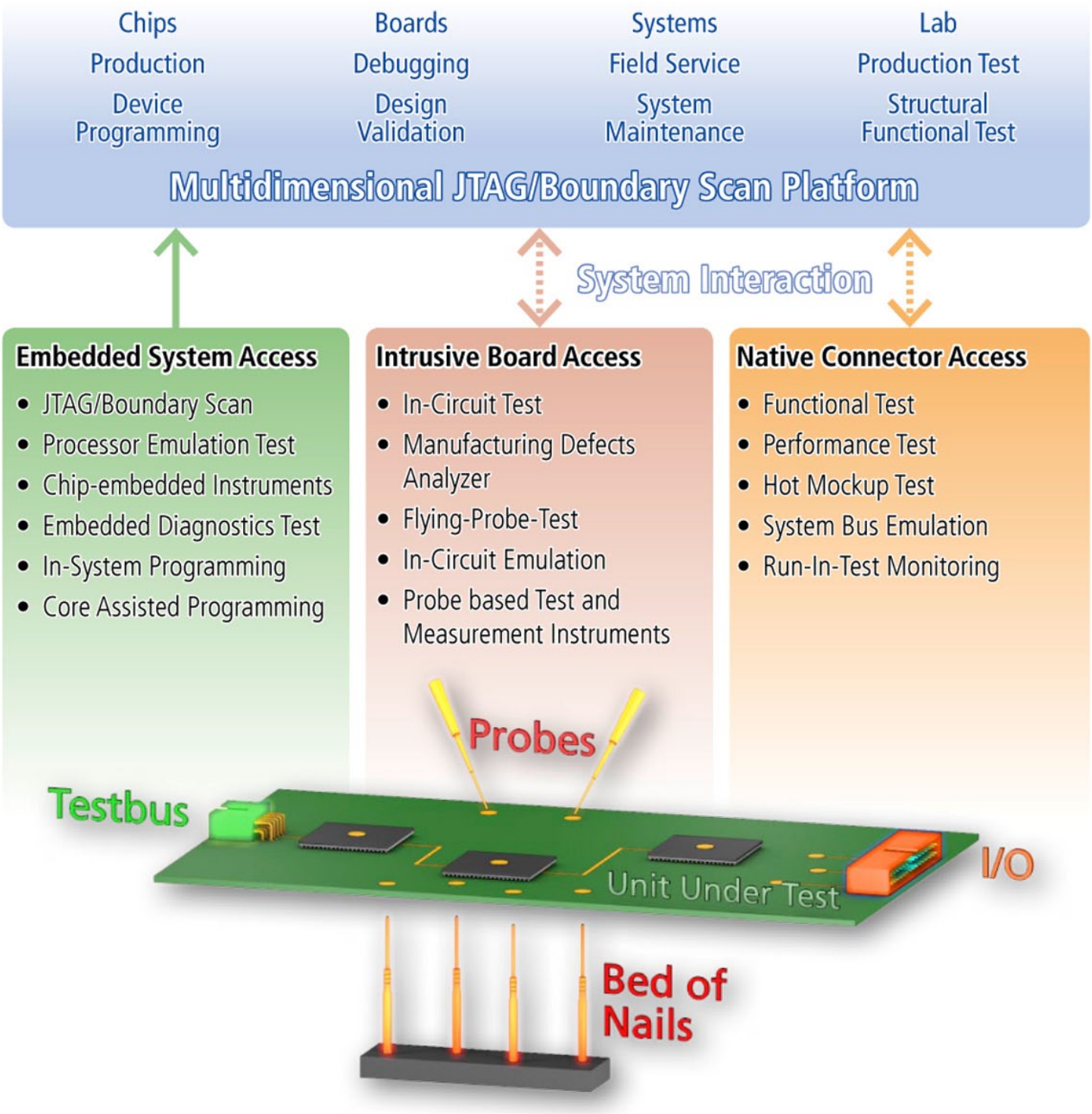

Figure 4 *Classification of the strategy of electrical access at board level*

the user gets a comprehensive insight into the circuitry to be tested and will see what the silicon sees. The JTAG test bus is used as transport medium for data and control commands. This bus is connected with a JTAG controller, which in turn is controlled with system software.

Basically, chip-embedded instruments are not a new invention as they have been used for years in chip test, for example in form of BIST IP. However, access to these instruments has not been standardised in the past, something that will be changed with the new standard IEEE P1687, which is currently under development; (IJTAG) [Reference 5], or IEEE1149.1-2012 [Reference 6].

FLEXIBILITY UNLIMITED

In particular, FPGA-embedded instruments, based on soft cores, have attracted strong interest recently. By enabling strategies such as FPGA assisted test (FAT) and FPGA assisted programming (FAP), they provide an enormous flexibility for the adaptation to individual test and measurement requirements. The idea is rather simple. Based on the circuit and the measuring task, a corresponding block of IP is uploaded into

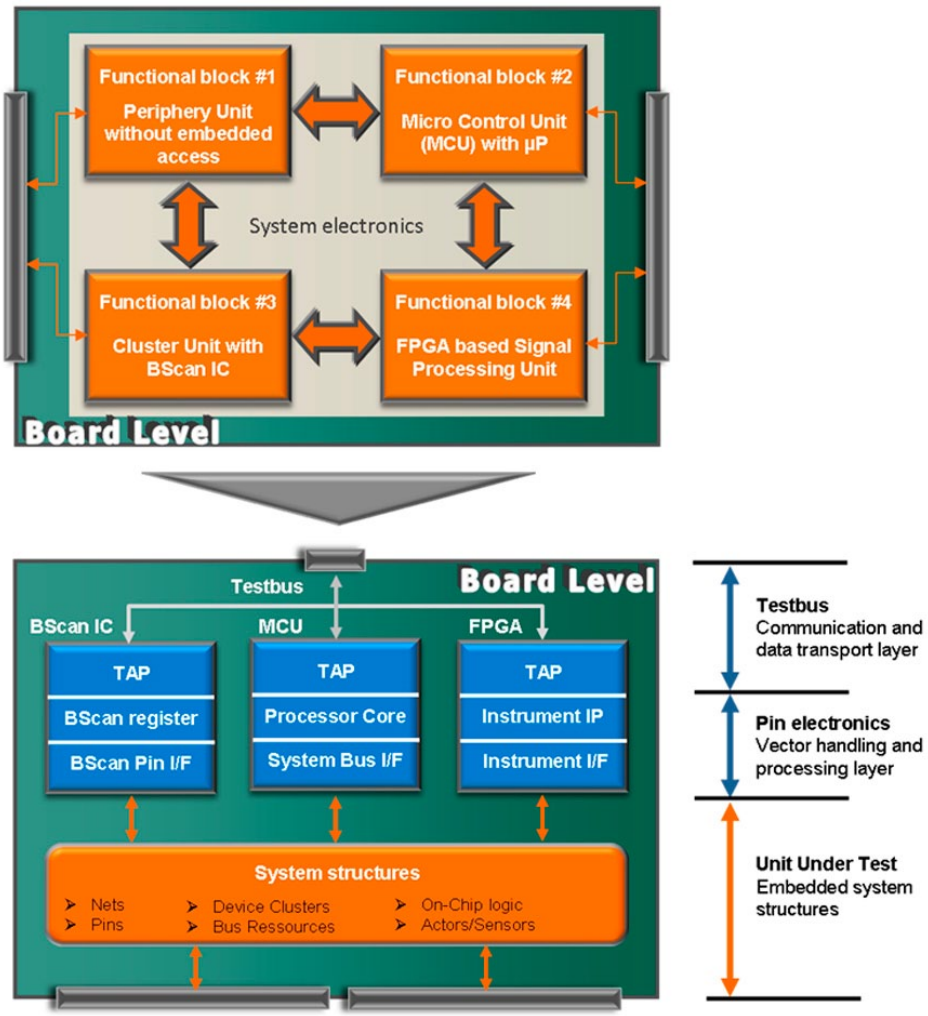

Figure 5 *Principle of transformation for use of Embedded System Access*

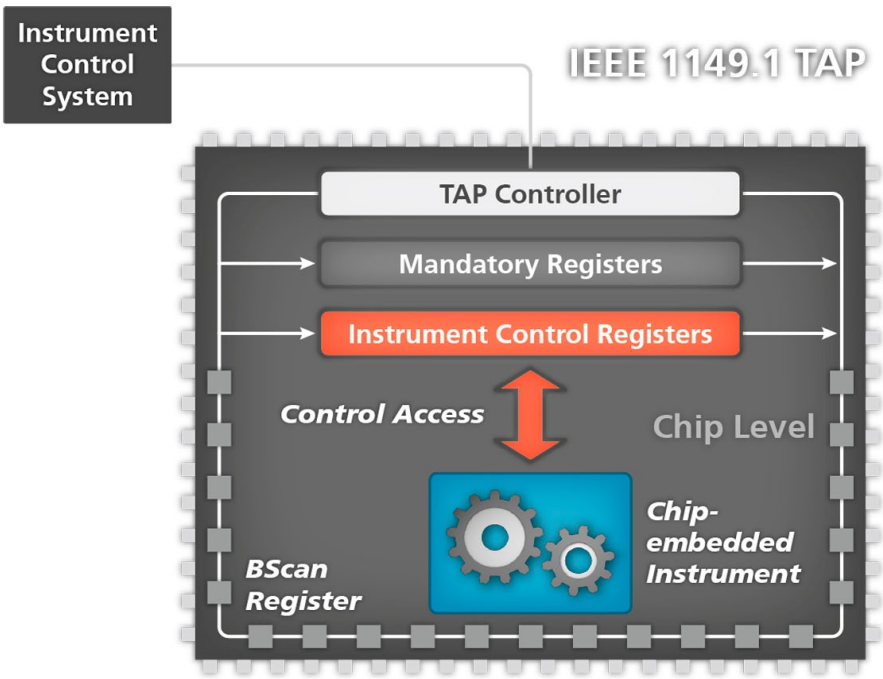

Figure 6 *Boundary scan IC includes chip-embedded instrument*

the target FPGA, configured, controlled, and finally removed again. Various test systems do exist that are capable of automating the handling of these processes. However, they differ in the method of IP generation. Basically it's all about how to join an existing IP to the corresponding signal pins (IP to Pin). Traditional systems require an extra synthesis run, which can be time-consuming and inflexible during interactive debugging.

At Goepel, we developed ChipVORX technology [Reference 7], which does not require synthesis runs and can be adapted to new tasks in a fraction of a second (see Figure 7). It relies on the same project database and the same runtime system as boundary scan.

ChipVORX comes with 300+ preconfigured intellectual property (IP) options and supports all common FPGA platforms for numerous applications such as RAM access test, frequency counter, BERT, or in-system programming of Flash memories. Compared with boundary scan, Flash programming runs up to 75 times faster and the RAM access test can reach a speed-up factor of 20. New IP is also available to support bit-error-rate tests. These instruments don't require synthesis and can be used for design validation (see Figure 8) and production test.

During production test, the bit error rate will be only checked for plausibility based on pre-defined setups, whereas during design validation the eye pattern can be graphically visualised as in Figure 9. This kind of visualisation is carried out directly in silicon and thus avoids the anomalies caused by tactile probing.

ESA OUTLOOK

The transition to ESA has begun a real paradigm shift in validation, test, programming, and debugging of complex electronic units. Within this context, more instruments are directly implemented in silicon or uploaded into FPGAs as soft macros, enabling designers to see exactly what the silicon sees.

New standards drive standardised access to these instruments and facilitate their use throughout the entire product life cycle. FPGA-embedded instruments are showing great promise. However, test systems must be capable of efficiently putting these possibilities into practice. In this respect, it is of paramount importance that innovative test and programming strategies can be run both stand-alone and in combination with intrusive test access methods such as in-circuit-test, on a common platform.

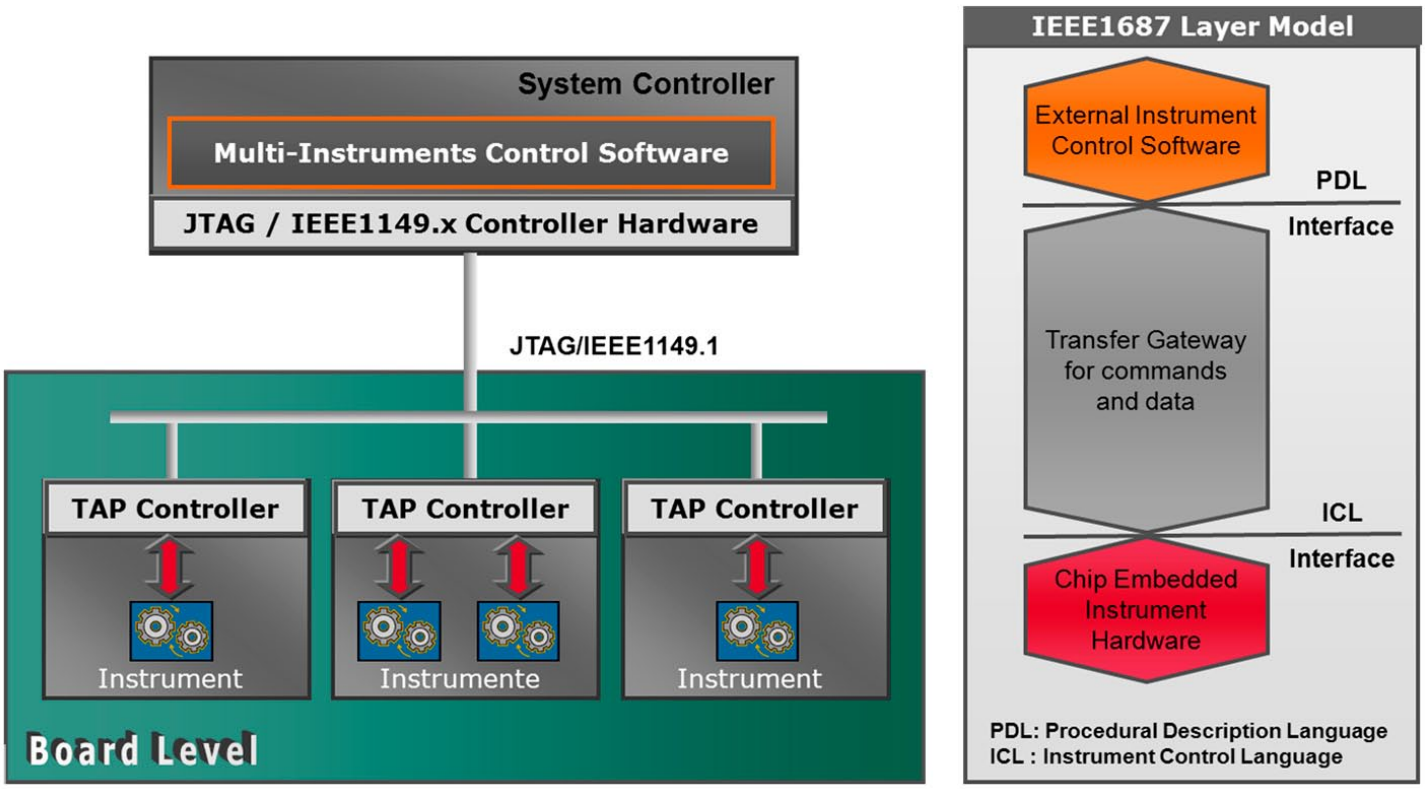

Figure 7 *ChipVORX uses automated IP handling*

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Thomas Wenzel is founding member and Managing Director of Goepel electronic GmbH in Jena, Germany, and is a foremost expert on the subject of boundary scan.

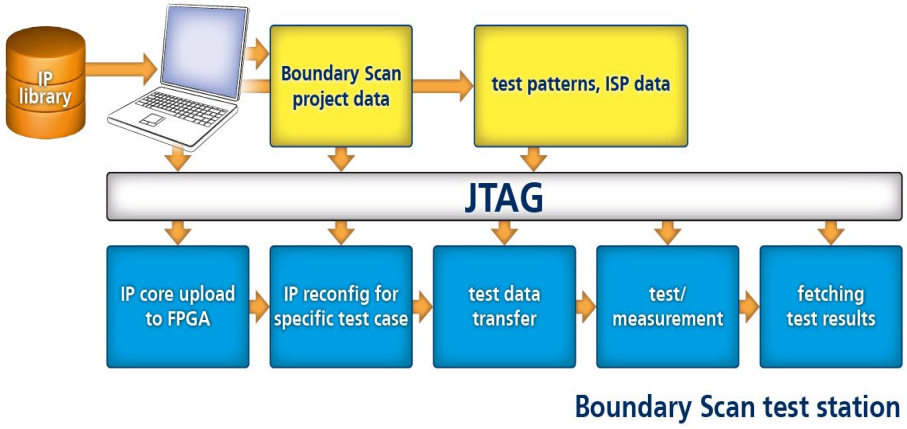

Figure 8 *Embedded instruments can be used for design validation and production test.*

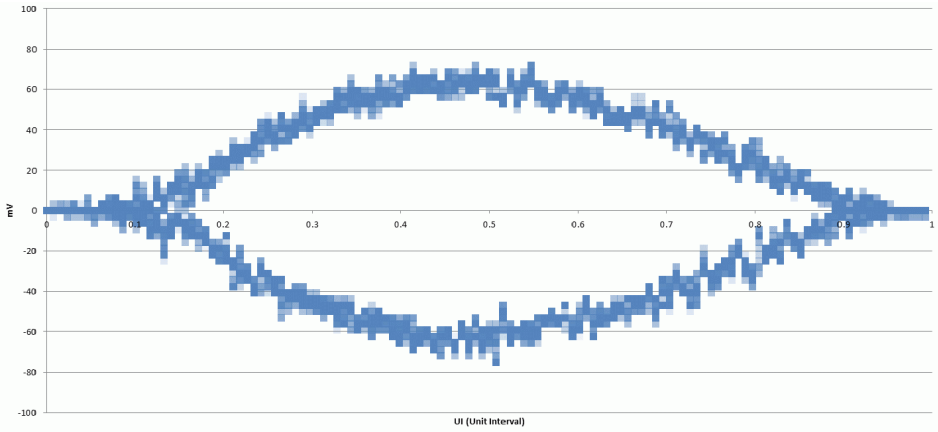

Figure 9 *Visualization of the eye pattern during FPGA Gbit link validation*

BY JACOB BENINGO • BENINGO ENGINEERING

10 SOFTWARE TIPS FOR HARDWARE ENGINEERS

HERE IS SOME ADVICE THAT I WISH I'D RECEIVED BACK IN THE DAY WHEN I WAS TRANSITIONING FROM HARDWARE TO SOFTWARE.

Embedded system design often requires an understanding of not only the hardware but also how the software affects and interacts with it. Designing hardware requires a certain engineering paradigm that can be the polar opposite of designing software. When transitioning from hardware design to include software design, here are 10 tips that hardware engineers should keep in mind.

TIP #1: FLOWCHART FIRST, IMPLEMENT SECOND

When an engineer first enters the realm of developing software, there is an intense temptation to jump right in and start writing code. This mind-set is the equivalent of trying to lay out a PCB before the schematics have been completed. It is critical when sitting down to develop software that the urge to start writing code be ignored and instead an architectural diagram of the software be developed using flowcharts. This approach will give the developer an idea of the different parts and components needed for the application, much like how a schematic tells an engineer what hardware components are required. Doing this step first ensures that the program overall will stand a better chance of being well organized and well thought out, which will save time and headaches in the long run by decreasing debugging time.

TIP #2: USE STATE MACHINES TO CONTROL PROGRAM FLOW

One of the great software inventions of the 20th century was the state machine. An application often can be broken up into multiple state machines, each of which controls a specific component of the application. Each of these state machines has its own internal states and state transitions that dictate how the software reacts to various stimuli. Designing software using state machines will ease the development of software that is modular, maintainable, and easy to understand. A wide variety of resources exist that demonstrate state-machine theory and algorithms.

WHEN DEALING WITH ANY COMPLEX TASK, THE SIMPLEST APPROACH IS TO BREAK IT UP INTO MORE MANAGEABLE TASKS.

TIP #3: AVOID THE USE OF GLOBAL VARIABLES

In the old days of functional programming, function came before form, with the programmer's only goal being to make the program operate as expected as quickly as possible without regard for program structure or reusability. This programming paradigm held no apprehension about using variables that were global in scope and that any function within the program could modify. The result was an increased chance of variable corruption or misuse of variables. In the new recommended object-oriented paradigm, variables should be defined in the smallest possible scope and encapsulated to prevent other functions from misusing or corrupting the variables. It is therefore recommended that you limit the number of variables that use a global scope. These variables can be identified in the C language by the use of the external keyword.

TIP #4: TAKE ADVANTAGE OF MODULARITY

If you ask any engineer what part of a project is most likely to be delivered late and over budget, the answer will be the software. Software is often complex and can be difficult to develop and maintain, especially if the entire application resides in a single file or multiple files that are loosely correlated. To ease maintainability, reusability, and complexity, it is highly recommended that the programmer take advantage of the modularity of modern programming languages and break common functionality into modules. Breaking the code up in this manner will allow the programmer to start building libraries of functions and features that can then be reused from one application to the next, thus improving code quality through continuous testing in addition to decreasing time and development costs.

TIP #5: KEEP INTERRUPT SERVICE ROUTINES SIMPLE

An interrupt service routine is used to interrupt the processor from the branch of code that is currently being executed in order to handle a peripheral whose interrupt has just been triggered. Whenever an interrupt is executed, there is a certain amount of overhead required to save the current program state, run the interrupt, and then return the processor to the original program state. Modern processors are much faster than they were years ago, but this overhead still needs to be taken into account. In general, a programmer wants to minimize the time spent in interrupts and so avoid interfering with the primary code branch. This means that interrupts should be short and simple. Functions should not be called from an interrupt. In addition, if an interrupt starts to get too complex or take too much time, the interrupt should be used to do the minimum required at the time, such as loading data into a buffer and setting a flag to then allow the main branch to process the incoming data. Doing this ensures that the majority of the processors' cycles are being spent running the application and not just processing interrupts.

TIP #6: USE PROCESSOR EXAMPLE CODE TO EXPERIMENT WITH PERIPHERALS

When designing hardware, it is always helpful to build prototype test circuits to make sure that an engineer's understanding of the circuit is correct before laying out a board. The same can be done when writing software. Silicon manufacturers usually have example code that can be used to test out parts

of the microprocessor so that the engineer can get a feel for how the part works. This approach allows insights to be made into how the software architecture should be organized and any potential issues that could be encountered. Identifying potential roadblocks early in the design process is preferable to finding them in the last hours before shipping a product. This is a great way to test out code snippets beforehand, but be warned that manufacturer code is usually not modular and easily used in the actual application without considerable modification. Over time, this limitation has been changing and may one day result in production-ready code right from the chip provider.

TIP #7: LIMIT FUNCTION COMPLEXITY

There is an old expression in engineering called KISS—Keep it simple, silly. When dealing with any complex task, the simplest approach is to break it up into smaller and simpler tasks that are more manageable. As tasks or functions become more complex, it becomes harder for humans to keep track of all the details without allowing errors to slip in. When a function is written, the complexity may seem appropriate at the time, but how an engineer will view the code when it needs to be maintained six months down the road should be considered. There are a number of techniques for measuring function complexity, such as cyclomatic complexity. Tools exist that can automatically calculate the cyclomatic complexity of a function. A general rule of thumb suggests that functions with a cyclomatic complexity below 10 are desirable.

TIP #8: USE A SOURCE-CODE REPOSITORY AND COMMIT FREQUENTLY

Making mistakes is part of being human, and when humans write code, they don't miraculously change. That's why it is critical that developers use a source-code repository. A source-code repository allows a developer to "check in" a good version of code with a description of what changes were made to the code base. This step allows the developer to not only revert or go back to an old version of code but also compare previous versions for changes. In the event a developer makes a number of changes that then break the system, going back to a good version of code is just a click away! Remember that if code is not committed frequently, the repository will not work as intended. Waiting two weeks to commit code and then going back will cause the loss of a lot of work and time if an irreversible change is made!

IF A DEVELOPER MAKES CHANGES THAT BREAK THE SYSTEM, GOING BACK TO A GOOD VERSION OF CODE IS JUST A CLICK AWAY!

TIP #9: DOCUMENT THE CODE THOROUGHLY

When in the heat of software-development battles, it is very easy to focus just on getting the code written and debugged and ignore the need to document it. Documentation often becomes an end-of-project task, as it is the last thing on a developer's mind when the pressure is on. It is important, however, to document the code when it is fresh in your mind so that a future developer or your future self can read the comments and understand how the code works.

TIP #10: USE AN AGILE DEVELOPMENT PROCESS

When doing engineering of any kind, it is always recommended that some sort of process be defined and followed. The result should be consistent quality and costs, as well as on-time delivery. Software developers have been successfully using the Agile development process to develop quality software. The process allows for requirements to be developed with priorities. The highest-priority tasks are performed first within a scheduled period of time known as an iteration. The beauty of the approach is that it permits the software-development process to be fluid, allowing requirements and tasks to adapt and change with each iteration based on the results and needs of the client.

Readers weigh in

"I don't agree with the advice on interrupt routines. When using a low-power microcontroller such as TI's MSP430, the main line code is often nothing more than putting the processor to sleep. All of the action takes place in the interrupt routine when the processor is awakened."—DickB

"From my experience, perhaps this should have been titled '10 software tips for software engineers.'
Once interviewed a software engineer for a new position and asked the question 'How do you go about writing software for a new project?'
The answer was 'Start coding the software'!
What I was expecting was 'Read the specifications,' followed by 'Break down the software into individual modules and flowchart them,' or something similar.
He didn't get the job."—The Real Dr Bob

"All very good. Would like to add 10b: Get rest of organization (management) educated on 'Agile' (and general compromises related to the other development processes).
Biggest 'truth' to be understood: setting realistic goals for the completion of the project while still at the beginning of the project (a recurring theme).
Another perspective on same subject: assigning appropriate manpower and processes at the beginning, not adding later, when things are late.
One 'man year' effort equals 720 people working a problem 'til lunch time? (Hard to kill this one.)"—Thinking_J

TIP #10A: STAY ON TOP OF DEVELOPING TECHNOLOGIES

A great place to learn about the latest tools and techniques being used to develop embedded software is one of the Embedded Systems Conferences, held twice a year, in San Jose, CA (www.ubmdesign.com/sanjose) and Boston (east.ubmdesign.com). These conferences draw engineers from around the world, providing the opportunity to interact, attend seminars, and try hands-on exercises that will improve their understanding of software development. In addition, the Community area of EDN.com offers a variety of blogs (www.edn.com/blogs) on hardware and software topics to keep engineers always engaged and learning so that they are ready to apply cutting-edge technologies in their next development project.**EDN**

AUTHOR'S BIOGRAPHY

Jacob Beningo is a Certified Software Development Professional (CSDP) who specializes in the development and design of quality, robust embedded systems. He has written technical papers on embedded design methods and taught courses on programmable devices, boot-loaders, and software methods. Beningo holds bachelor's degrees in engineering and physics from Central Michigan University (Mount Pleasant, MI) and a master's degree in space-systems engineering from the University of Michigan (Ann Arbor, MI).

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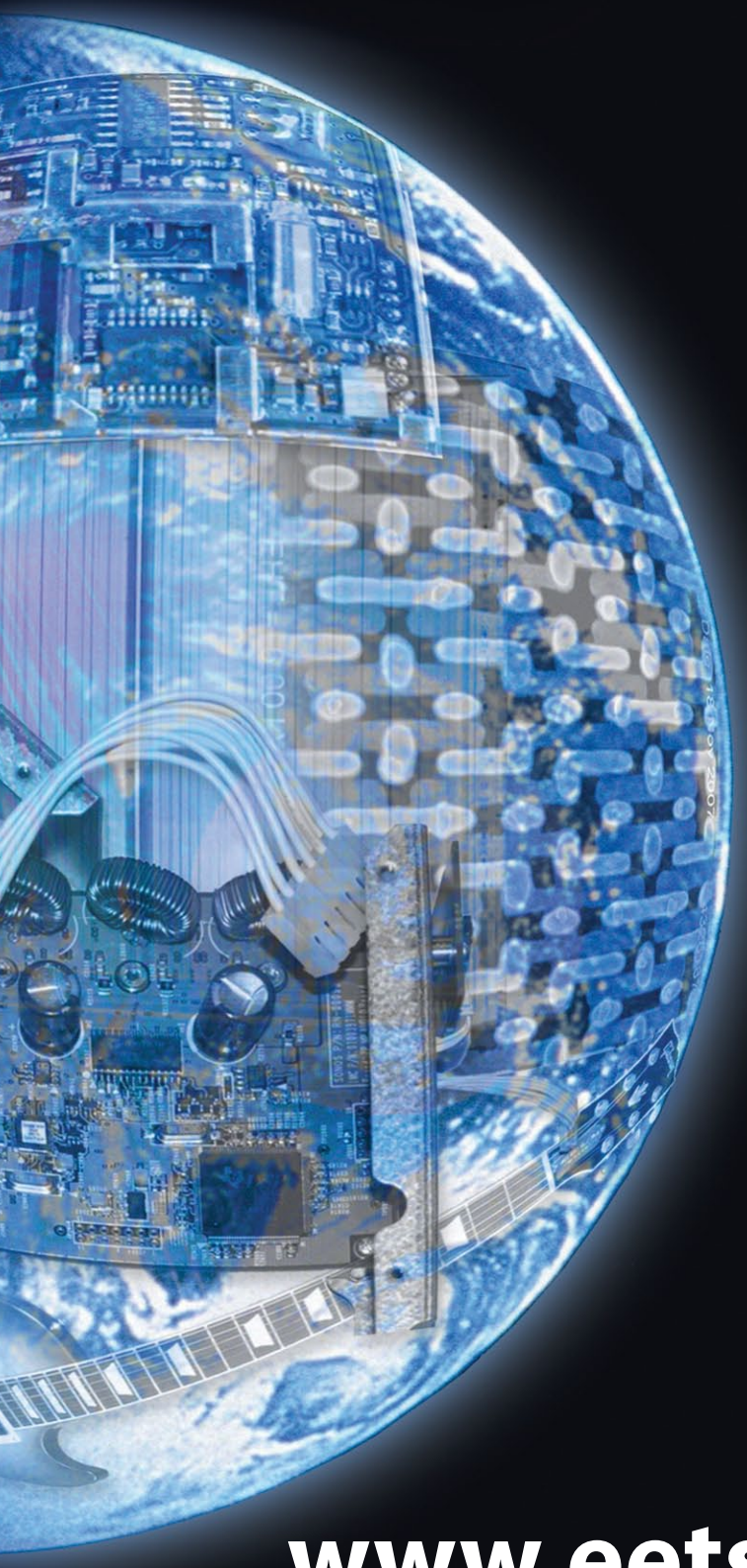

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READERS SOLVE DESIGN PROBLEMS

Recover the leakage energy of a flyback transformer

Todor Arsenov, Spellman High Voltage Electronics Corp, Hauppauge, NY

DIs Inside

The classical technique for demagnetizing the transformer in any forward converter is to implement a second winding bifilar with the primary winding to ensure continuous flow of the magnetizing current when the power switch (typically a power FET) turns off. Such a circuit generally limits or clamps the FET's drain-to-source voltage to two times the dc supply-rail voltage. The same technique—using this recuperating winding—can be successfully implemented in a flyback topology to deal with the leakage-inductance problem.

Note that in any flyback converter, the flyback transformer (multiwinding inductor) is far from perfect; leakage inductance (primary to secondary) is as much as 5% of the magnetizing primary inductance [1]. The leakage inductance (LLK) is effectively in series with the power FET (drain connection). Complicating matters, the parasitic output capacitance of the FET (COSS) forms a series-resonant circuit with LLK. When the FET turns off, very high overvoltage and ringing can occur. The higher the Q of the circuit, the higher the ringing voltage. This situation will likely cause significant EM interference and, due to the elevated FET drain voltage, lower the FET reliability.

Figure 1a shows a flyback converter with such a recuperating winding added on a modified demonstration board (STMicroelectronics' Viper17L [2]). Some important considerations: Resistors RS1 and RS2 are sense resistors used for monitoring the currents; scope measurements for currents are measured directly across these resistors. The transformer ratios are the same as in the original transformer. The recuperating winding, NR, is magnetically coupled tightly to only the primary winding, NP, by making these two windings bifilar. Bifilar windings are made by simultaneously winding two wires side by side around the magnetic core, or bobbin; this approach maximizes coupling and tightly matches the parasitic capacitance and inductance. The coupling between the primary and the other windings is not as important.

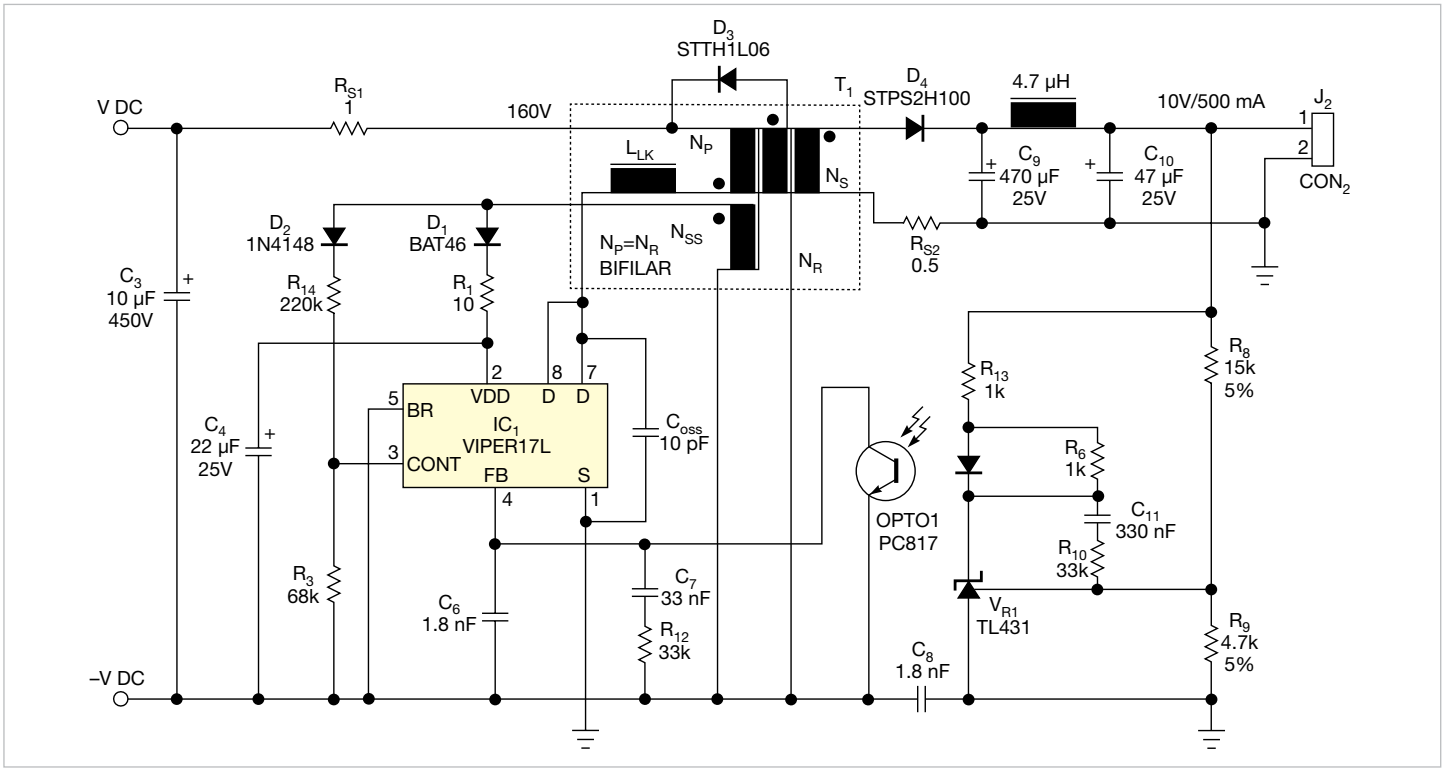


Figure 1a *A passive snubber is realized by adding a bifilar winding, NR, and a diode, D3, to a flyback transformer.*

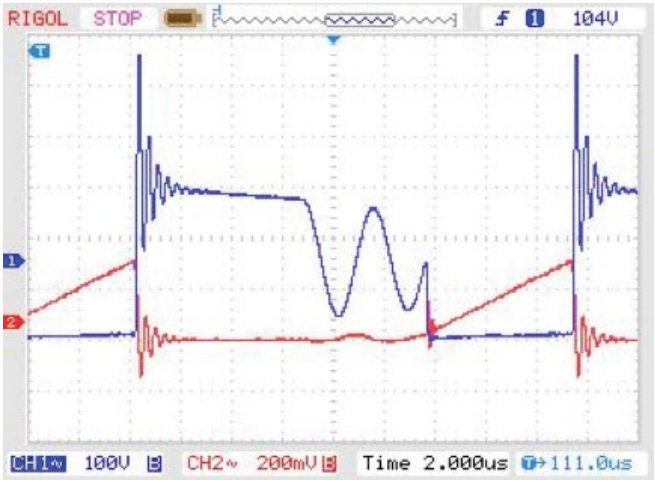


Figure 1b *Without any snubbers, the ringing on voltage (Channel 1, blue) and current (Channel 2, red) waveforms can be quite big.*

In Figure 1b, it can be seen that without any clamping (D3 disconnected), the voltage at the FET's drain (IC1, pins 7 and 8) due to the ringing reaches 560V peak. The primary current is shown magnified in Figure 2a. At the moment the FET turns off, the primary current (magnetizing current) remains constant, charging the capacitance, COSS. This is indicated by the step waveform. The magnetizing current remains constant, as diode D4 on the secondary side is still not conducting; this can be seen from the secondary current waveform in Figure 2b. The short period of time after the turn-off (when D4 is not yet conducting) is the time when the series-resonance circuit's COSS is charged. Corresponding to the time when the FET's drain voltage, VDS, becomes high enough, D4 becomes forward biased and the energy stored in the series-resonant tank circuit is released. The energy stored is a function of the resonant circuit's Q factor and is surprisingly high.

When the recuperating winding, NR, and diode D3 are connected to the power-supply rail, a completely different process is observed. The recuperating winding simply bypasses the parasitic COSS, steering the accumulated leakage energy back to the supply rail. In Figure 2c, it should be noted that the nega-

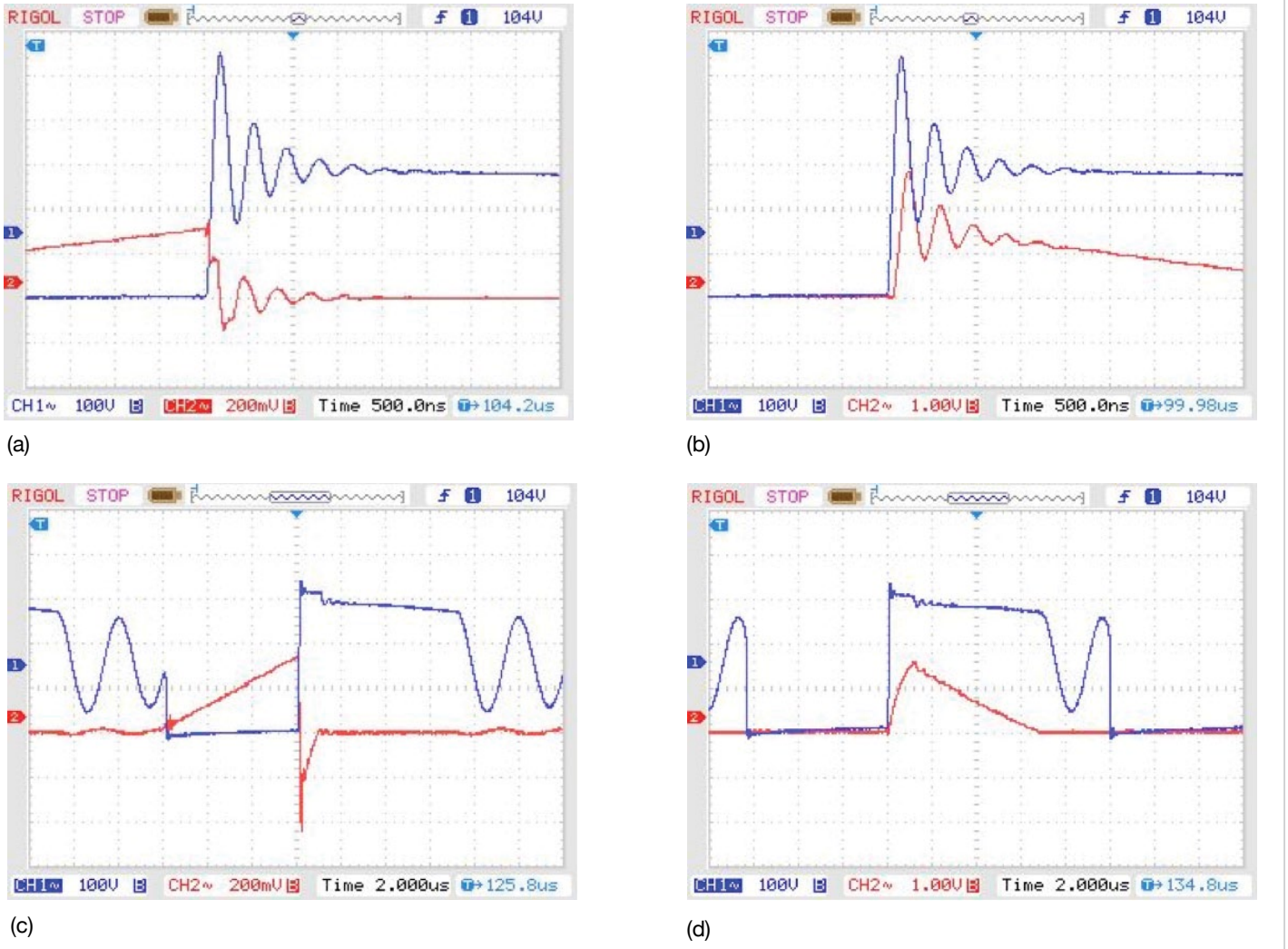


Figure 2 *In these results from the series tank circuit, there is ringing at the FET's drain (VDS, Channel 1, blue) after the primary current (Channel 2, red) charges COSS following turn-off (a). VDS is again shown as Channel 1; the charging of COSS delays the secondary current through D4 (Channel 2) by just under 100 nsec (b). The bifilar winding, NR, steers the primary current (Channel 2) back to the power rail and clamps the switch voltage (Channel 1) (c). The leakage flux fights the current transfer; the secondary current (Channel 2) rises to an equilibrium peak value until the leakage energy is fully recuperated (d).*

tive surge of the primary current (Channel 2) is actually the current flowing from the recuperating winding. The secondary diode, D4, is forward biased immediately (Figure 2d); as the secondary current (Channel 2) rises to the steady-state peak value, the primary current diminishes to zero. As NP=NR, this assures limiting of the VDSS to two times VDC.

Eliminating the excessive ringing by leakage-energy recuperation is clearly an advantage as all other passive RCD snubber techniques dissipate this energy and thus lower the efficiency of the converter. Limiting the maximum VDS to two times VDC is acceptable bearing in mind that most monolithic embedded converters incorporate high-voltage power FETs. (STMicroelectronics' Viper17, for example, has an impressive 800V rugged power section [3]. Bifilar windings are readily available from most of the transformer vendors, or, for in-house production, a Multifilar magnet wire can be used to make these windings.**EDN**

REFERENCES

1 Dixon, Lloyd H, Magnetic design handbook, Texas Instruments, 2001.
2 "EVALVIPER17L-7W demonstration board," STMicroelectronics, June 2008, http://bit.ly/145jGHF.
3 "VIPER17 data sheet," STMicro-electronics, June 2010, http://bit.ly/Z8xOqM.

Double the protection of a laser driver using a 1V power supply

Tai-Shan Liao, National Applied Research Laboratories, Instrument Technology Research Center, Hsinchu, Taiwan

An excessive level of light from a laser pointer, even if only for a short duration, can be harmful if it enters the human eye either directly or through reflection from a shiny object. Most countries, therefore, have laser safety requirements that limit the maximum emission level. This Design Idea describes a laser driver that works even with a single 1.5V cell discharged to 1V, and uses dual current-control transistors to improve reliability against shorting and allowing excessive laser current and light emission.

In Figure 1, the transistors Q1, Q2, and Q3 compose a negative impedance, which can be described approximately as Z≈–β(VDD–VBE)/RF. Assume that all of the transistors have the same current gain (β), and VBE is the base-to-emitter voltage of all transistors. Feedback is provided through RF, and R1 bias controls the collector current of Q1. Inductor L1 and parasitic capacitance form a resonant circuit that oscillates due to the negative impedance, resulting in about 3.5V pk-pk at Q1's collector, with the battery at 1V. Schottky diode D1 and C1 form a half-wave rectifier that provides about –3V for the laser cathode; with VDD at 1V, this provides a 4V working range to overcome the laser threshold.

Q5 and Q6 control the laser current. The photodiode built into the laser assembly monitors the light intensity and sends negative feedback through Q4 to bias Q5 and Q6 to the proper collector current for the constant desired laser intensity. The Q5 and Q6 pair is series connected so that if one should fail shorted, the other will still maintain the laser current at a safe level. The probability of failure of two transistors at the same time is far lower than the probability of failure of a single transistor.

Editor's note: Due to variations in laser and photodiode efficiency, R7 might need to be adjusted to ensure the laser output is within safety-regulation limits. **EDN**

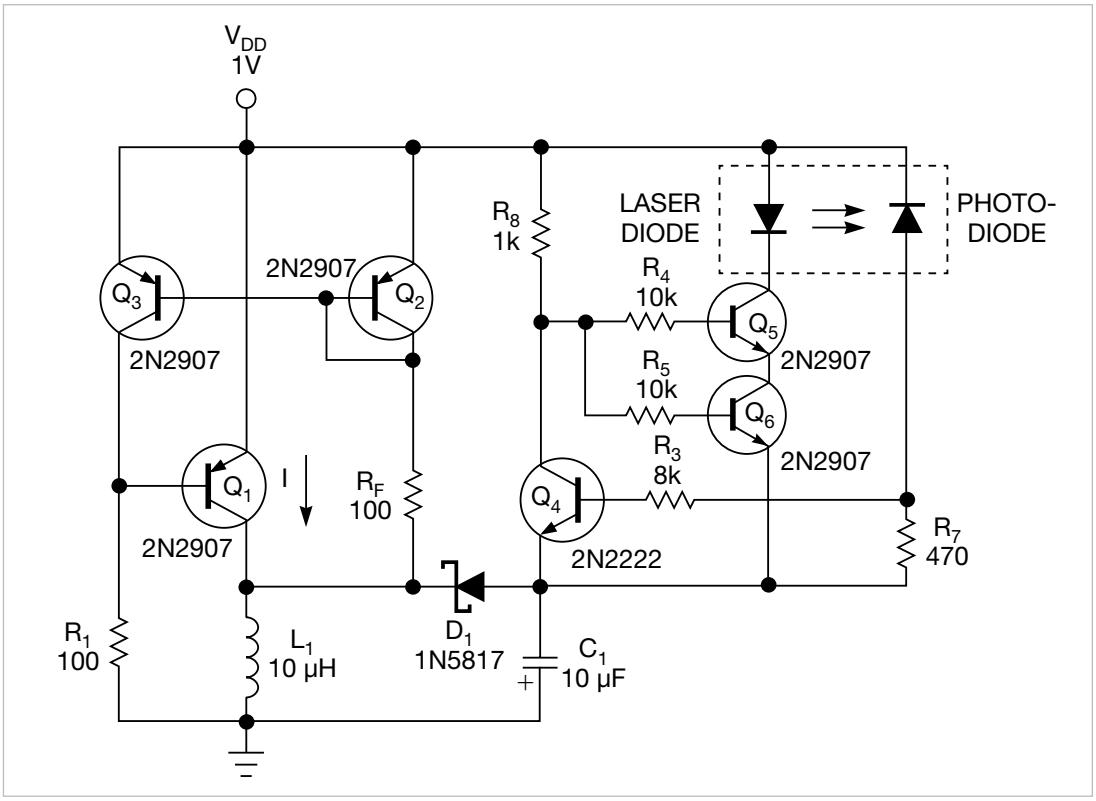


Figure 1 *You can use this dc-dc step-up circuit and dual current-control transistors to safely power this laser from an almost-discharged battery.*

Gate-drive transformer eases multi-output, isolated dc/dc-converter designs

Robert N Buono, Crestron Electronics Inc, Rockleigh, NJ

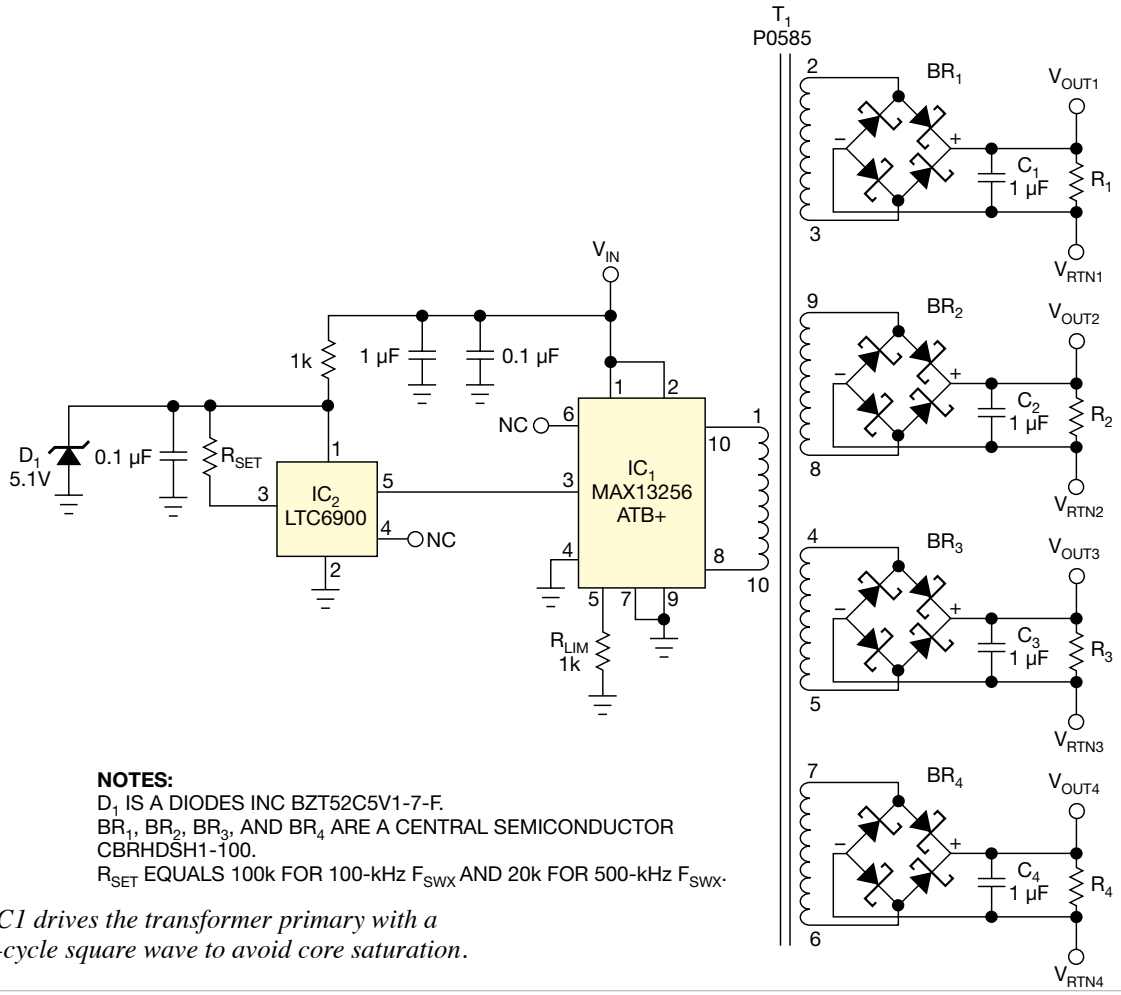
Oftentimes the biggest obstacle in designing an isolated dc/dc converter is the transformer design, a prospect that sometimes discourages designers from undertaking an otherwise straightforward design task. You can take advantage of the characteristics of an off-the-shelf gate-drive transformer and produce four separate isolated dc outputs. Gate-drive transformers are actually ideal for low-power dc/dc power transfer, because they have already been optimized for a high product of voltage and time (ET, or volt-microsecond, product) as well as for low leakage inductance.

A core with high permeability and low core loss at high switching frequency (FSWX) supports the typical 10 to 15V applied primary voltage and the typical 500-nsec to 5-µsec on-time of switching frequencies between 100 and 500 kHz. This range of voltage and time is in the range needed for this dc/dc design. Also, a core geometry and winding configuration has already been chosen for low leakage inductance in order to produce fast rise and fall times, as well as low ringing. Lastly, the wire gauges used are sufficient for dc/dc-converter applications handling winding currents in the tens-of-milliamps range without excessive copper losses.

The Pulse Electronics P0585 gate-drive transformer has five windings, each with an identical number of turns [1]. One winding is wound with triple-insulated wire (TIW); the other four windings are standard magnet wire. You drive the TIW winding as the primary to provide a 3-kVRMS primary-to-secondary breakdown rating. The breakdown voltage rating between the four secondary windings is not specified, but this type of wire insulation is typically used in offline supplies where up to 400V can be seen between windings.

Isolated outputs offer great flexibility. They provide a convenient way to break ground loops, power remote circuits at different ground potentials, and allow for simple negative or positive output voltage polarity selection. Figure 1 shows the four secondaries of this transformer, creating four separate, equal-voltage outputs. You can, however, wire these secondaries in various series/parallel combinations to produce a myriad of output voltage/current combinations.

The Maxim MAX-13256 H-bridge transformer driver (IC1) is an ideal part for this application. It incorporates all of the functions needed for a standalone,



NOTES:
D_1 IS A DIODES INC BZT52C5V1-7-F.
BR_1, BR_2, BR_3, AND BR_4 ARE A CENTRAL SEMICONDUCTOR CBRHDSH1-100.
R_{SET} EQUALS 100k FOR 100-kHz F_{SWX} AND 20k FOR 500-kHz F_{SWX}.

Figure 1 *IC1 drives the transformer primary with a 50%-duty-cycle square wave to avoid core saturation.*

transformer-isolated dc/dc converter. Its internal FETs withstand 36V and are configured as two separate push-pull outputs, which drive a transformer primary with a precise 50% duty cycle to avoid core saturation. It also incorporates adjustable and robust internal current limiting, so the outputs are protected against short circuits and recover nicely upon fault removal. It also incorporates undervoltage lockout (UVLO) to prevent switching activity when the input voltage is too low.

The Linear Technology LTC6900 clock source (IC2) was added to allow precision adjustability of the switching frequency. The MAX13256 does have an internal clock, but most users would probably prefer to set the switching frequency themselves for overall system compatibility or EMI reasons. The MAX13256 accepts an external TTL-level clock, and its UVLO feature ensures that IC2 is up and running before the ramping VIN of IC1 reaches its turn-on threshold. The value of RSET determines the output frequency of IC2, which is set to twice the desired switching frequency of IC1.

Table 1 shows the measured results for 10, 12, and 15V input voltages at switching frequencies of 100 and 500 kHz. Due to the high switching frequency, low leakage inductance, and use of Schottky bridge rectifiers, the outputs produce very low voltage ripple of less than 20 mV pk-pk, even with low-value (1 µF) surface-mounted ceramic output capacitors. The table also shows the efficiency as well as the output voltage versus load current variation due to the outputs being unregulated. The outputs could be followed by linear regulators if lower noise or more tightly regulated dc outputs are desired.

For these measurements, full load is the loading that produces a measured primary current of 500 mA peak. This is the minimum current-limit threshold for the MAX13256 when RLIM is 1 kΩ. Some designers may want to operate at less than these empirically determined full-load current levels for more margin against spurious overcurrent tripping. The light-load output voltage rise observed with the higher switching frequency is due to the fact that this is a snubber-less design for simplicity and high efficiency. As the switching frequency rises, more leakage inductance energy is generated, which transfers to the secondary windings and increases the measured output voltages.

Following is a brief tutorial on checking the transformer operating parameters against the data-sheet specifications. The P0585 transformer has a maximum ET product of 95 Vµsec. This calculation is the product of the maximum voltage impressed across the primary winding and the maximum time that voltage is present (on-time). Since the MAX13256 drives the transformer primary with a precise 50% duty cycle, the maximum ET product will occur with a 15V input voltage. At the lowest switching frequency of 100 kHz in this case, the maximum on-time at 100 kHz is 5 µsec. The maximum ET product is therefore 75 Vµsec, which meets the specification.

The peak flux-density spec is 2100 Gauss. To calculate peak flux density, equations 2A and 2B provided on the data sheet are based on VIN and the switching frequency. Again, peak flux density is produced under operating conditions of VIN=15V and a 100-kHz switching frequency. Note that in equation 2A, "DON" is the duty cycle of 50%, or 0.5, not time in microseconds. Under these conditions, the calculated peak flux density is 1512 Gauss, which meets the data-sheet specification.

Core loss is calculated using the formulas provided on the transformer data sheet. The results are 0.468W at 100 kHz and 0.117W at 500 kHz, which is lower than at 100 kHz due to the lower ET product.

The copper loss of 93.75 mW was calculated using the formula provided on the transformer data sheet. This simplified formula calculates copper loss based on I^2R losses in the windings and does not consider skin or proximity effects in the windings. Therefore, there is no frequency dependence in these simplified results, which are based on ±500-mA peak current in the primary winding and ±125-mA peak currents in each of the four secondary windings.

Using the temperature-rise formula from the transformer data sheet and the total losses calculated above (561.75 mW at 100 kHz), the predicted temperature rise of the transformer is 37.2°C.

This Design Idea uses the P0585 gate-drive transformer, but other (smaller) off-the-shelf gate-drive transformers can be used, especially if fewer outputs are needed, and at less current. Just be sure to check the transformer's maximum volt-µsec specification as in the example described here. **EDN**

REFERENCE

"P0585 transformer data sheet," Pulse Electronics, http://bit.ly/ZVsWYb.

TABLE 1 MEASURED RESULTS AT INPUT VOLTAGES OF 10, 12, AND 15V DC

Switching frequency	Measurements	V_{IN}=10V DC	V_{IN}=12V DC	V_{IN}=15V DC
100 kHz	V_{OUT} at I_{OUT} (light load)	9.82V at 1.31 mA	11.82V at 1.58 mA	14.77V at 1.97 mA
	V_{OUT} at I_{OUT} (full load)	8.19V at 110.29 mA	10.26V at 103.97 mA	13.17V at 111.51 mA
	P_{OUT} at full load (each output, total)	0.9W, 3.61W	1.07W, 4.27W	1.47W, 5.87W
	I_{IN}, P_{IN} at full load	450.4 mA, 4.5W	428.28 mA, 5.14W	463.33 mA, 6.95W
	Efficiency (P_{OUT}/P_{IN}) at full load	80.22%	83.07%	84.46%
500 kHz	V_{OUT} at I_{OUT} (light load)	12.92V at 1.72 mA	15.3V at 2.04 mA	18.74V at 2.5 mA
	V_{OUT} at I_{OUT} full load)	8.09V at 108.94 mA	10.2V at 103.36 mA	13.12V at 111.08 mA
	P_{OUT} at full load (each output, total)	881 mW, 3.53W	1.05W, 4.2W	1.46W, 5.84W
	I_{IN}, P_{IN} at full load	445.45 mA, 4.45W	426.26 mA, 5.12W	461.72 mA, 6.93W
	Efficiency (P_{OUT}/P_{IN}) at full load	79.33%	82.42%	84.13%

productroundup

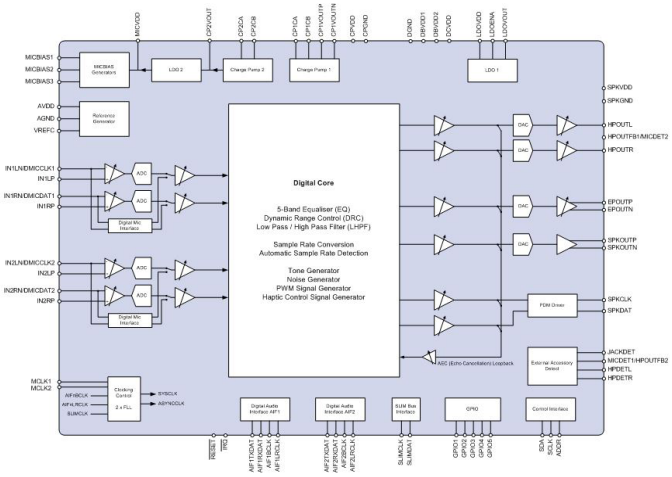
Integrated op amps on 8-bit PIC MCUs

Microchip Technology has introduced two 8-bit PIC microcontrollers, the PIC16F527 and PIC16F570, which add low-cost analogue peripherals to create a well-integrated, cost-effective family suitable for a wide range of applications. With an on-chip dual Op Amp module, 8-bit ADC and two comparators, these MCUs are suitable for systems that require signal conditioning and amplification to interpret analogue inputs. The PIC16F527 and PIC16F570 employ a small and efficient 8-bit architecture, and add several features to support ease of use and system robustness. The new hardware interrupt capability gives designers the freedom to implement more complex functions without adding software overhead, while an integrated Brown-Out Reset (BOR) can detect faults in system power and safely reset the MCU to avoid memory corruption. The two MCUs also feature self-read/write programme Flash memory, which allows for high-use data EEPROM functionality.

Microchip, www.microchip.com/get/JB5A

HD Audio hub with SLIMbus and I²S

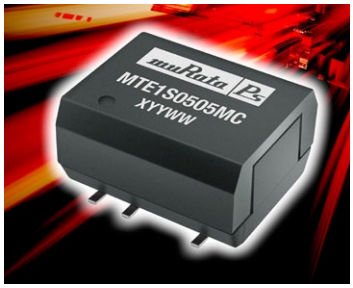
Wolfson Microelectronics' WM8997 is a flexible High Definition (HD) Audio Hub with simultaneous SLIMbus and I²S interfaces designed to provide HD Audio for smartphones and other portable devices in a cost-effective solution. The Hub delivers 102 dB signal-to-noise ratio (SNR) at 6.5 mW DAC to headphone playback power consumption. Its simultaneous SLIMbus and I²S functionality provides platform architecture flexibility enabling standalone audio digital signal processors (DSPs) and ensures that the same audio solution can be re-used across any platform irrespective of the audio interface, saving development costs and time, and delivering an easily-integrated, future-proof solution. The WM8997 digital core combines fixed-function signal processing blocks, including filters, equalisers, dynamic processors and sample rate converters, with a fully-flexible, all-digital audio mixing and routing engine. It also enables the use of voice and gesture control, as well as a digital stylus. The WM8997 supports up to four microphone inputs, each either analogue or pulse density modulation (PDM) digital.



Wolfson, www.wolfsonmicro.com

88% efficient 1-Watt DC-DC converter

Murata Power Solutions' MTE1 series of isolated 1-Watt single output DC-DC converters offers efficiency up to 88%, with better efficiency across the full load range than competitor models, and with higher reliability rates. The MTE1 series also has a load regulation that is typically 5% better than similar models. Input voltage options are the five most popular nominal input voltages of 3.3, 5, 12, 15, or 24 VDC input. Output voltages include 3.3, 5, 9, 12, or 15 VDC. Full load capability is provided across the full industrial temperature range of -40C to +85C. The MTE1 series has the highest moisture sensitivity level rating, MSL 1, and is compatible with a peak reflow solder temperature of 245C as per J-STD-020D. Packaged to match an industry standard footprint, the MTE1 series can be used as a pin-compatible replacement for older designs without the need to re-engineer an application's PCB layout.



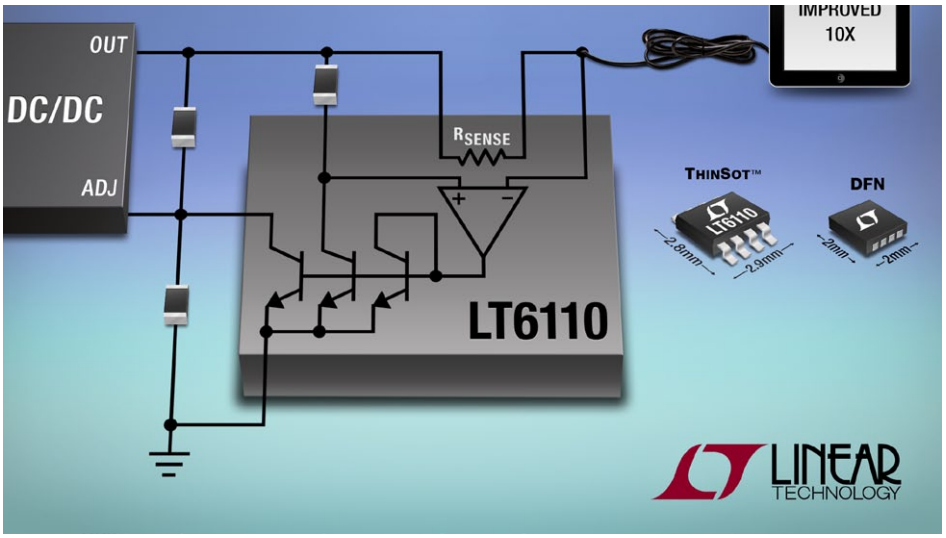
Murata Europe, www.murata.eu

Step-down switching regulators with built-in power MOSFET

Rohm Semiconductor has announced a series of step-down switching regulators with a built-in 45V/800-mΩ power MOSFET. The BD9G101G series provides 0.5A DC output with good line and load regulation for smart power management in a small SOT23 (SSOP6) package. The operating frequency is fixed at 1.5 MHz, allowing the use of a small inductor and a ceramic capacitor in order to reduce space requirements. All phase compensation components are integrated. The input voltage can vary from 6 to 42V, the internal reference voltage is set to 0.75V with an accuracy of typical ±1.5%. For step-down switching designs, the new device offers low thermal resistance and multiple protection features such as internal over-current protection, under-voltage lockout and thermal shutdown. The operating temperature is from -40°C to +105°C while the maximum junction temperature is 150°. Use them in industrial distributed power and automotive applications, battery powered equipment and medical OA instruments.

Rohm, www.rohm.com/eu

Cable drop compensator replaces sense wires



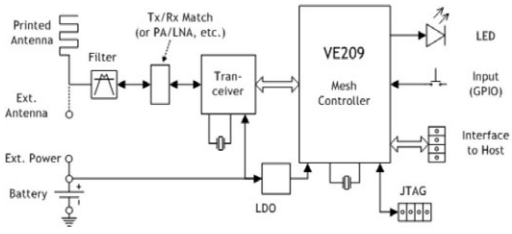
Linear Technology's LT6110 cable drop compensator improves voltage regulation at remote loads without the need for Kelvin sense wires. You can use it with most types of voltage regulators for which it can provide several volts of load regulation compensation. The LT6110 will compensate for the voltage drop due to resistance in a wire, circuit board trace or cable and can improve regulation at the load by a factor of 10. It operates with supply voltages that range from 2V to 50V, making it suitable for high power USB, Power over Ethernet (PoE), remote instrumentation and remote industrial applications. The LT6110 reduces costs by eliminating sense wires which may be prone to misconnection or damage and it makes load regulation independent of wire size or length.

It operates by measuring the load current with a single sense resistor and injecting current into the existing regulator's feedback loop to raise the output voltage. It is designed to work with standard feedback circuits, as well as "current source" reference devices. For load currents less than 3A, the internal 20 mOhm sense resistor simplifies the design. For higher currents, an external sense resistor is used. Wide bandwidth achieves fast transient compensation of load steps, and in most cases the savings in wire and labour outweigh the cost of the LT6110. Maximum input offset voltage is 300µV ; output current accuracy is 1% max; supply current is 30µA max; and the chip operates from a supply of 2V to 50V. It costs $1.29 (1,000)

Linear Technology, www.linear.com/product/LT6110

Sub-GHz energy harvest mesh networks

Microsemi and Virtual Extension, Israel have collaborated to produce what they claim to be the lowest-power mesh networking chipset available. The two-chip wireless mesh network chipset and reference design offers performance and signal robustness in applications requiring networks with high performance and ultra-low power consumption. The reference design features Microsemi's ZL70250 chip scale package (CSP) radio frequency (RF) transceiver for industrial, scientific and medical (ISM) band applications and Virtual Extension's VE209M wireless mesh controller. The combination provides system engineers with an ultra-low power, high-performance solution to build wireless sensing networks with no single point-of-failure and robust operation for energy-harvesting powered or battery-operated wireless mesh applications. The ZL70250 CSP is an ultra low power RF transceiver operating in the unlicensed frequency bands between 795 and 965 MHz and delivers a data rate of 186 kbits/sec at 2 mA current to transmit and receive data, enabling extremely long battery life or permitting energy harvesting wireless sensor networks.

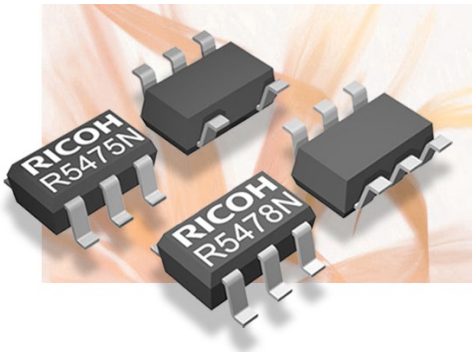


Block Diagram of a typical VEmesh node using VE209

More; www.microsemi.com and www.virtual-extension.com

Li-Ion/Li-Polymer battery protection chips

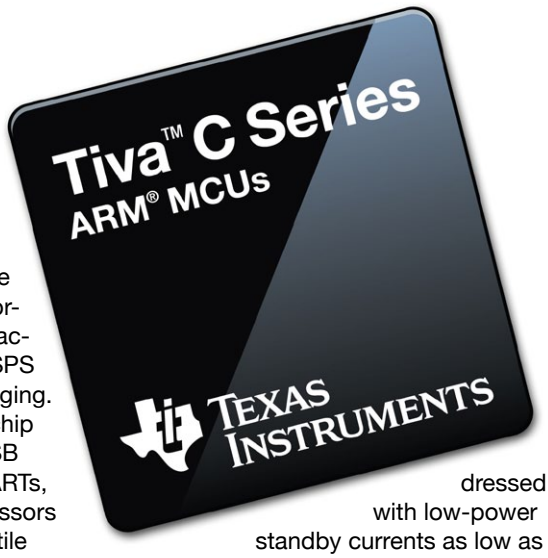
Ricoh Europe has launched two 1-Cell lithium-ion/lithium polymer battery protection ICs, the R5475 and R5478, for use in rechargeable portable electronic products, providing safety measures for the charge and discharge process in order to assure failsafe operation of the battery pack. The IC monitors the charge and discharge process and intervenes as soon as the process is at risk of going beyond the safe operation range of the battery cell. The protection ICs can be used on the application circuit board, or integrated in a laminated battery pack. The R5475 and R5478 offer standard detection circuits for example, over-charge voltage, over-discharge voltage, excess-discharge current and short protection. As soon the over-charge voltage threshold is exceeded, the chip will interrupt the charge process preventing an overload condition. In the event that the over-discharge voltage threshold is exceeded, the chip will interrupt the discharge process, entering into a standby mode lowering the current consumption and ensuring further discharge is kept to a minimum.



Ricoh, www.ricoh.com/LSI

Stellaris becomes Tiva, extends ARM Cortex-M4 MCUs

In the processor series formerly known as Stellaris, Texas Instruments has introduced Tiva C Series ARM Cortex-M4-based MCUs, offering connectivity and sensor aggregation, along with tools and software for development. The first devices in the new platform – Tiva C Series TM4C123x ARM Cortex-M4 MCUs – are the first Cortex-M-based MCUs to be built on 65-nm flash process technology, enabling higher speeds, larger memory and lower power. The MCUs target varied applications with ARM Cortex-M4 floating-point core, operating at up to 80 MHz; they support mixed-signal applications with high-performance analogue integration – two high-performance 12-bit analogue-to-digital converters (ADCs) and three comparators. They eliminate performance tradeoffs with 12-bit ADC accuracy, achievable at the full 1 MSPS rating without any hardware averaging. The chips communicate with on-chip connectivity options, including USB (host, device and On-The-Go), UARTs, I²C, SSI/SPI and CAN. TIVA processors support high-endurance non-volatile storage of user interface or configuration parameters to reduce system cost using integrated EEPROM. Longer battery life and constrained power budgets are addressed with low-power standby currents as low as 1.6 µA. Memory options include up to 256 kB flash and 32 kB SRAM.

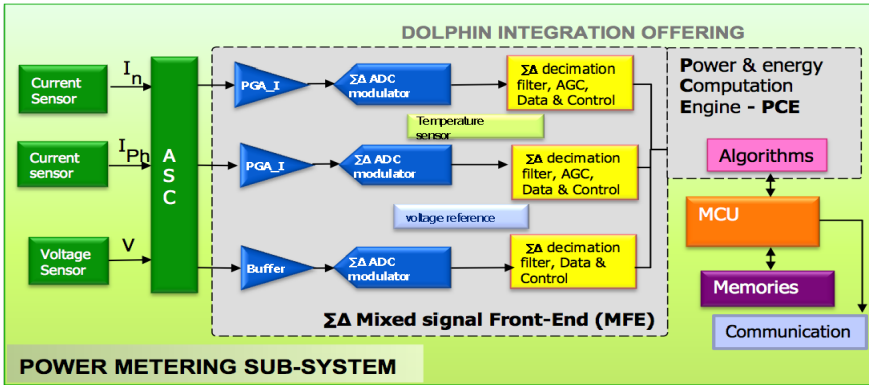


TI, www.ti.com

Interface box connects GPIB, USB, and RS-232 test instruments to LAN

Agilent Technologies' E5810B LAN/GPIB/USB gateway is an upgrade of the E5810A with added USB capability. The new gateway allows you to connect and control, over a standard local-area network, up to 14 GPIB instruments, up to four USB instruments via a self-powered hub, and an RS-232 instrument. With the gateway's improved GPIB transfer rate of 1.2 MB/sec, the E5810B supports 1000BASE-T (1 Gigabit) LAN/Ethernet as well as 100BASE-TX and 10BASE-T to meet the demands of higher network bandwidth. The E5810B comes with a built-in LCD display, allowing users to check the IP address of the gateway for quick setup. It allows multiple users in different locations to access a centrally located test system. Connecting a wireless router to the E5810B enables engineers to wirelessly control instruments from a PC where LAN connection is unavailable or inconvenient. You can use it for system integrations, shared test systems in R&D, design verification and manufacturing environments.

Agilent; www.agilent.com/find/E5810B_pr



Complete IP offering for power metering applications

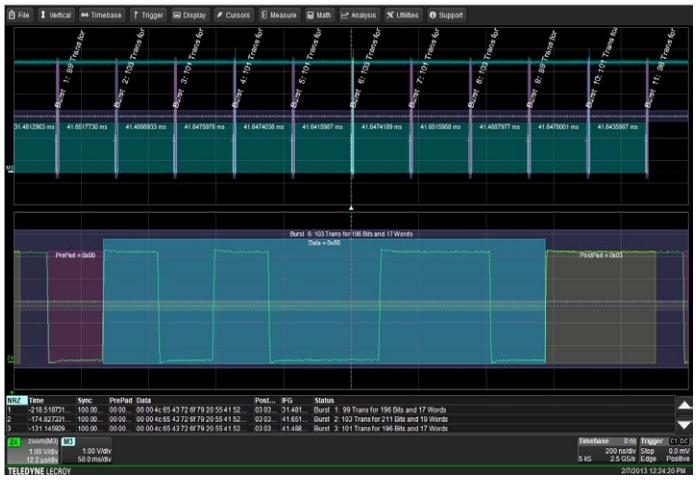
Grenoble-based silicon-intellectual property (IP) specialist Dolphin Integration is introducing a complete subsystem for Smart Grid applications: the first Silicon IP combining a mixed-signal front end (MFE) with a power and energy computation engine (PCE). The IP enables a metering product to achieve class 0.1% at the system-level with several sensors while targeting a measurement range up to 1/10,000. The Dolphin solution optimises trade-offs between MFE and PCE and ensure performance as good as 0.05% accuracy at SoC-level. To simplify integration, the analogue front-end (AFE) is augmented with a range of peripherals: temperature sensor, low-drift voltage reference and the relevant embedded power management, ensuring immunity to noise and cross-talk.

The MFE converts real-time sensor signals into serial digital figures for current and voltage.

PCE computes a range of derived values (Line frequency, Irms, Vrms…), energy consumption in real time and its cumulative value. The MFE features; 20-bit and 21-bit Delta-Sigma ADCs ; measurement accuracy of 0.05% over a range of 1:5,000 for 250 µOhm shunt with 21-bit MFE, to 1:10,000 for a current transformer with 20-bit MFE with its automatic gain controller; supported sensors of both shunt and current transformer type; low drift voltage reference; temperature sensor; low noise regulator.

Dolphin; www.dolphin.fr/flip/analog/measure/analog_metro_PM_Jade_mono.05.html

Scope protocol decoders for Manchester and NRZ coding



LeCroy - now Teledyne LeCroy - has announced Manchester and NRZ (non-return-to-zero) configurable protocol decoders for a wide range of oscilloscope platforms. The decoders enable users to specify a broad range of physical layer characteristics for Manchester- or NRZ-encoded signals. The decoders define the grouping of bits into words, and words into frames, which simplifies analysis for custom and/or proprietary protocols based on those generic encoding schemes. Decoded information is then shown in a colour-coded overlay directly on top of the physical layer waveform. Teledyne LeCroy's Manchester and NRZ protocol provide broad flexibility in terms of physical layer characteristics, protocol word and frame structure as well as other parameters. Users may specify bit rates from 10 bits/sec to 10 Gbits/sec. Idle states, sync bits, header and footer information can all be configured to decode custom preambles or CRC details. Decoding is highly flexible: data mode can be in bits or words; viewing in hex, ASCII, or decimal; and bit order may be either LSB or MSB.

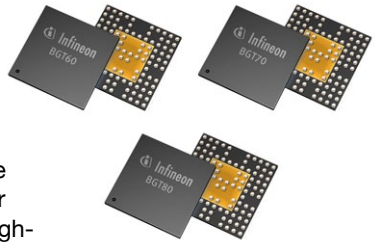
LeCroy, www.teledynelecroy.com

Designing and verifying embedded state machines

Version 7.1 of IAR visualSTATE adds extensive features for state machine-based design and formal verification. IAR Systems has released a new version of its state machine tool suite IAR visualSTATE. The version adds several new features and integrations to simplify development of complex state- or event-driven embedded systems. IAR visualSTATE allows users to build their design from a high level, structure complex applications, step by step add functions in detail, and automatically generate code that is 100% consistent with the design. It also provides advanced formal verification, analysis and validation that can be used to make sure the applications behave as intended. IAR visualSTATE is integrated with the C/C++ compiler and debugger tool suite IAR Embedded Workbench. When using the tools together, full state machine debugging on hardware is available. IAR Systems also provides a free-standing Viewer for IAR visualSTATE users.

IAR, www.iar.com/vs

SiGe transceivers for mm-wave wireless backhaul



Infineon has introduced a family of single-chip transceiver ICs that simplify design of small cell backhaul links, easing system design and production logistics by replacing more than 10 discrete devices. Due to their low power consumption the single-chip high-integration transceivers also help to reduce fixed expenses in high data rate millimeter wave wireless backhaul communication systems. The new transceivers address the market for wireless data links with data rates of more than 1 Gbps between LTE/4G base stations and core networks. The BGTx0 family provides a complete radio frequency (RF) front-end for wireless communication in 57-64 GHz, 71-76 GHz, or 81-86 GHz millimeter wave bands. Paired with a baseband/modem, the system solution requires less space, offers improved reliability and lower cost for the critical wireless backhaul links needed in mobile base stations that support LTE/4G networks. RF performance of SiGe (silicon-germanium) technology includes deliverable output power up to 18 dBm of PA, low noise figure of 6 dB of LNA and VCO phase noise better than -85dBc/Hz at 100 kHz offset – allows a system designer to implement high modulation schemes up to QAM64 with a sample rate of 500 Msamples/sec and QAM32 with 1Gsamples/sec at a 10^{-6} BER (Bit Error Rate).

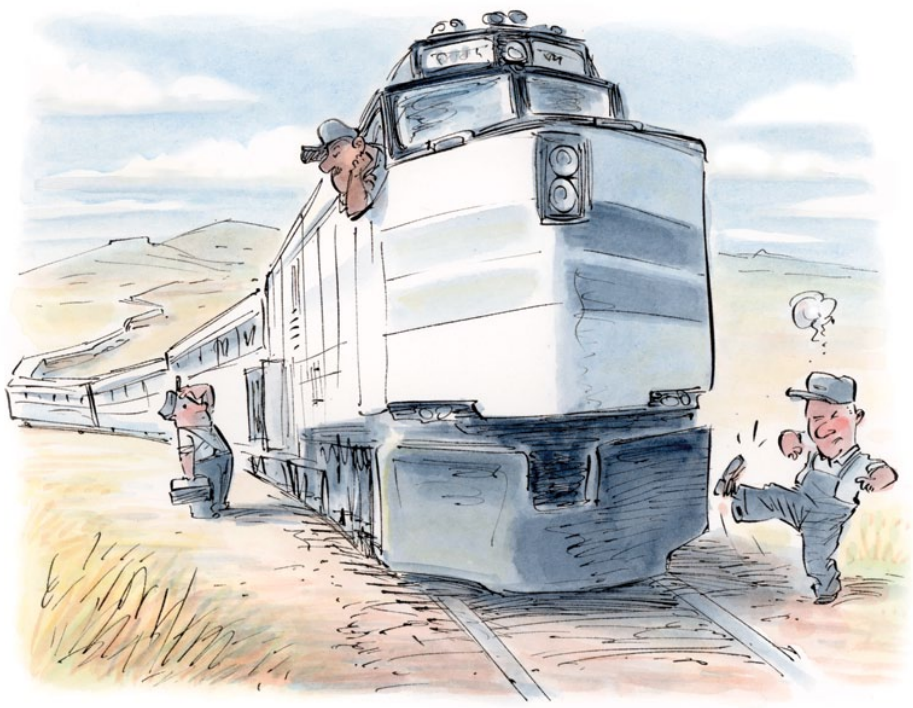
Infineon; www.infineon.com/backhaul

Single point tuneable colourLED lighting array

The Tiger Zenigata LED array is presented as the first single point light source to feature 'tuneable' colour temperature output, enabling light output colour to be smoothly adjusted to optimise comfort, productivity and well being. Ismosys, Sharp Microelectronics' pan-European sales and marketing representative, is sampling the latest addition to the company's Zenigata family of chip-on-board (COB) LED lighting arrays. The Tiger Zenigata LED module features independently controllable intermeshed 'stripes' of yellow (cool) and orange (warm) phosphors (hence the 'Tiger' derivation). 168 blue LED chips are coated by strips of different blends of red and green phosphors, which create the warm or cold white light components. A dual-channel LED driver is used to independently adjust the output of each LED 'stripe' and so changes the overall colour temperature output of the array. The circuit for the 2700K 'stripe' is made up of 96 chips arranged in eight parallel strips of 12 LEDs. The 5700K 'stripe' is created from 72 chips in six parallel strips. Each 'stripe' needs a forward voltage of 37V at a maximum power supply of 700 mA.

Ismosys, www.ismosys.com

Decoupling caps are where it's at



The company I had transferred to in the Midwest back in the 1980s made locomotives and was plagued by a long-term field problem. An overcurrent-protection circuit would sometimes trip when the locomotive controller was cold. This situation posed a serious problem for operation of the locomotive, because if the engine lost power, trains would not be able to operate and pull reliably, and the locomotive engine became a million-dollar paperweight.

A unit exhibited the problem at the factory in the rail yard, and the assembly crew gladly brought the controller back to the engineering lab for evaluation. The box was ice-cold and displayed the apparent overcurrent condition. Test engineering fired up the automated test procedure and quickly trapped the fault.

The design was set up so that the microprocessor would select an analog-to-digital channel to read back, and then read back the value for scrutiny. The problem here was the value coming back was much too high too high, and was equivalent to reading back many, many more amps on the traction motors than desired.

Closer inspection showed that the selected channel was being written satisfactorily by the microprocessor but wasn't getting held reliably by the latch. Inspecting the power-supply (VCC) lines to the chip showed a dip in the supply coincident with the write of the register. So the analog-to-digital channel we thought we were reading was not the intended one.

The board layout showed a long VCC trace from the decoupling capacitor to the IC before being stitched down to the VCC plane. The dip in the VCC caused the latch/register IC—some multi-D-latch variety of the 74ALS374, if you remember the pre-VLSI days, called MSI (medium-scale integration) days—to lose "consciousness." When VCC returned, the latched address value was scrambled and was pointing to the wrong analog-to-digital channel to be read.

A product from Rogers Corp, which I came across while reading some trade literature, provided the solution to this problem. Rogers made a nifty device that mounted right below the DIP and inserted nicely under the existing IC package. We quickly obtained samples, tacked them piggyback-style onto the tops of the offending latch, and then watched the VCC droop diminish well within limits. The latch could remain functional during the microprocessor write, and the system could read back the correct channel. Multiple quick fixes later, we had our solution without having to re-lay out the board! Because we had found the root cause, the test results and field repairs went smoothly and quickly.

Packaging technologies have changed, but decoupling capacitors are the reason every electronic design can actually function. If you don't believe me, try to build a board without any decoupling caps and send me the scope photos of the VCC lines near ICs!

A PRODUCT FROM ROGERS CORP PROVIDED THE SOLUTION. THE NIFTY DEVICE MOUNTED RIGHT BELOW THE DIP AND INSERTED NICELY UNDER THE EXISTING IC PACKAGE.

So the lesson learned was that the VCC and grounds must be fed and cared for judiciously, or all hell will break loose. In addition, I swore to myself that going forward I would never design a system where you can write but not read back a register to verify the write. In some ways it reminded me of the write-only memory, but with much worse consequences. (Throughout my career, I have accumulated a few of these principles and collectively refer to them as, well, Maxim's maxims.) **EDN**

Maxim "Jay" Skender has been an electronic design engineer, for both analog and digital (FPGA and embedded microprocessor) applications, for most of his 28 years in the industry. He received a bachelor's degree in electrical engineering from California Polytechnic State University (San Luis Obispo, CA) in 1985.

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